



# MAX9601 Evaluation Kit

## General Description

The MAX9601 evaluation kit (EV kit) is a fully assembled and tested surface-mount PCB that evaluates the MAX9601 dual-channel PECL output comparators. It can be used to evaluate the MAX9601's performance in tracking high-fidelity narrow pulses, as well as conform its low-propagation delay and delay dispersion. The differential input stage accepts a wide range of signals in the common-mode range from (VEE + 3V) to (VCC - 2V). The outputs are complementary digital signals with external components necessary to observe the PECL serial-data output on a 50Ω input oscilloscope. The board also provides layout options that allow the output termination to be modified easily for alternate output terminations, such as +5V PECL and high impedance or AC-coupled level translation. The EV kit features test points to control the complementary latch-enable control inputs. The EV kit also provides resistor footprints to evaluate the MAX9601's adjustable hysteresis feature.

## Features

- ◆ -2.2V to +3V Input Range with +5V/-5.2V Supplies
- ◆ -1.2V to +4V Input Range with +6V/-4.2V Supplies
- ◆ SMA Connectors to Access Differential Inputs and Outputs
- ◆ Differential PECL Outputs
- ◆ Latch Enable
- ◆ Adjustable Hysteresis
- ◆ Output Terminated for Interfacing with a 50Ω Oscilloscope Input
- ◆ Allows Alternate Output Terminations
- ◆ Fully Assembled and Tested

## Ordering Information

PART	TYPE
MAX9601EVKIT+	EV Kit

+Denotes lead(Pb)-free and RoHS compliant.

## Component List

DESIGNATION	QTY	DESCRIPTION
C1, C13, C17, C22	4	0Ω ±5% resistors (0603)
C5, C8, C11, C20	4	10μF ±10%, 10V X7R ceramic capacitors (1206) Murata GRM31CR71A106K TDK C3216X7R1A106K
C6, C9, C12, C19	4	0.1μF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H104K TDK C1608X7R1H104K
C7, C10, C18, C21	4	0.01μF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H103K TDK C1608X7R1H103K
INA+, INA-, INB+, INB-, QA, QA, QB, QB	8	Edge-mount receptacle SMA connectors

DESIGNATION	QTY	DESCRIPTION
LEA, LEA, LEB, LEB	4	Test points
R1, R4, R10, R13	4	4.53Ω ±1% resistors (0603)
R2, R3, R11, R12	4	82.5Ω ±1% resistors (0603)
R6, R8, R9, R15, R17, R18	6	49.9Ω ±1% resistors (0603)
R7, R16	2	16.5kΩ ±1% resistors (0603)
R19–R22, R27–R30	8	90.9Ω ±1% resistors (0603)
U1	1	Dual PECL high-speed comparator (20 TSSOP) Maxim MAX9601EUP+
—	1	PCB: MAX9601 EVALUATION KIT+

Evaluates: MAX9601

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## Component Suppliers

SUPPLIER	PHONE	WEBSITE
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com
TDK Corp.	847-803-6100	www.component.tdk.com

**Note:** Indicate that you are using the MAX9601 when contacting these component suppliers.

### Quick Start

#### Recommended Equipment

- DC power supplies
  - +5V, 100mA positive power supply (VCC)
  - 5.2V, 100mA negative power supply (VEE)
  - +5V, 100mA logic power supply (VCCO<sub>-</sub>)
  - +3V 1mA latch enable power supply (LE<sub>-</sub>)
- RF signal generator (e.g., MAX8685A)
- High-bandwidth oscilloscope

#### Procedure

The MAX9601 EV kit is fully assembled and tested. Follow the steps below to verify board operation.

**Caution: Do not turn on power supplies until all connections are completed.**

- 1) Set the VCC power supply to +5V. Disable VCC.
- 2) Connect the negative terminal of the VCC power supply to the GND pad. Connect the positive terminal of the VCC power supply to the VCC pad.
- 3) Set the VEE power supply to -5.2V. Disable VEE.
- 4) Connect the negative terminal of the VEE power supply to the VEE pad. Connect the positive terminal of the VEE power supply to the GND pad.
- 5) Set the VCCO<sub>-</sub> power supply to +5V. Disable VCCO<sub>-</sub>.
- 6) Connect the negative terminal of the VCCO<sub>-</sub> power supply to the GND pad. Connect the positive terminal of the VCCO<sub>-</sub> power supply to the VCCOA pad. Short the VCCOA pad to the VCCOB pad.
- 7) Set the LE<sub>-</sub> power supply to +3V. Disable LE<sub>-</sub>.
- 8) Connect the negative terminal of the LE<sub>-</sub> power supply to the GND pad. Connect the positive terminal of the LE<sub>-</sub> power supply to the LEA pad. Short the LEA pad to the LEB pad.
- 9) Set the signal generator to produce an output sine-wave signal of 100mV<sub>P-P</sub> at a frequency of 250MHz. Disable the signal generator.
- 10) Connect the signal generator to the edge-mount SMA connector marked INA<sub>+</sub>.
- 11) Enable all power supplies. Enable the signal generator.

12) Monitor and verify outputs QA and  $\overline{QA}$  with the oscilloscope. The oscilloscope must be configured for 50Ω input termination.

13) Monitor and verify outputs QB and  $\overline{QB}$  with the oscilloscope. The oscilloscope must be configured for 50Ω input termination.

### Detailed Description of Hardware

#### Supply Voltages

The MAX9601 EV kit operates from either standard supply levels of -5.2V/+5V or shifted levels of -4.2V/+6V. Connect the positive and negative supply voltages to the VCC and VEE pads, respectively. The EV kit also requires an output driver positive supply for each channel. Connect the logic supply voltages to the VCCOA and VCCOB pads.

#### Inputs

The EV kit provides INA<sub>+</sub>, INA<sub>-</sub>, INB<sub>+</sub>, and INB<sub>-</sub> SMA connectors to access the MAX9601's differential inputs. The differential input stage accepts a wide range of signals in the common-mode range from (VEE + 3V) to (VCC - 2V) with a CMRR of 70dB (typ). All the input traces are symmetrical and have 50Ω of characteristic impedance. Each input trace has a 49.9Ω termination resistor to avoid signal reflections.

#### Outputs

The EV kit provides QA,  $\overline{QA}$ , QB, and  $\overline{QB}$  SMA connectors to access the MAX9601's comparator outputs. All the output traces are symmetrical and have 50Ω of characteristic impedance. The output signals are referenced to the logic supply voltage VCCO<sub>-</sub> and have the external components necessary to observe the PECL output. See the *Output Termination* section for more details.

#### Hysteresis

Hysteresis can be introduced to prevent oscillation or multiple transitions due to noise on low-slew input signals. The EV kit features resistors R7 and R16 to program the current-controlled hysteresis. Refer to the *Hysteresis (MAX9600/MAX9601)* section in the MAX9601 IC data sheet for a more detailed description.

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## Latch Enable

The complementary latch-enable control permits tracking, track-hold, or sample-hold modes of operation. The latch enables can be driven with PECL logic. See Table 1 for the latch-enable truth table. By default, the EV kit is configured to operate in compare mode.  $\overline{LEA}$  and  $\overline{LEB}$  are connected to the VCCOA and VCCOB pads through resistors R6 and R15 (LEA and LEB signals need to be provided externally).

## Output Termination

### DC-Coupled Output to Oscilloscope

The EV kit's default output termination network provides the output with a Thevenin equivalent of  $50\Omega$  to VCCO<sub>-</sub> - 2V, when connected to a  $50\Omega$  load to ground. Hence, the outputs can be conveniently connected directly to an oscilloscope's  $50\Omega$  input. The termination network provides a 4x output signal attenuation. If only one of the serial-data outputs is connected to an oscilloscope, ensure that the other is still properly terminated. Keep in mind that the resistor networks at each output provide proper termination only when they are terminated through  $50\Omega$  to ground.

### AC-Coupled Output to Oscilloscope

The output can also be AC-coupled to the next stage. While AC-coupling the output, remember that the IC has an open-emitter output. Hence the output must have a DC path provided with suitable external pull-down resistors. Also, the resultant current sourced by the output stage must not exceed the output current capability of the part. For example, to AC-couple the QA output to a  $50\Omega$  input oscilloscope, short resistor R19. Replace resistor R2 with  $125\Omega$  and R27 with  $187.5\Omega$ . This provides a DC Thevenin equivalent of  $75\Omega$  to VCCO<sub>-</sub> - 2V. Now replace resistor R1 with  $49.9\Omega$  resistor and populate capacitor C1 with a suitable low-loss, high-frequency capacitor. With good coupling, the AC load adds an additional 8mA of output current only, since capacitor C1 blocks the DC component of the PECL output.

Table 1. Latch-Enable Truth Table

LATCH-ENABLE INPUT		OPERATION
LE <sub>-</sub>	$\overline{LE}$	
0	1	Compare mode (output follows input state)
1	0	Latch mode (output latches to last known output state)
0	1	Invalid condition (output is in unknown state)
1	0	

## Alternative PECL Output Termination

Alternative PECL output termination methods can be used for different logic interfaces as long as they provide a DC Thevenin equivalent of  $50\Omega$  to VCC - 2V. For example, to interface QA with a PECL or high-impedance input, short resistors R1 and R19, and replace R27 with a  $124\Omega$  resistor. To interface QA with a PECL input test equipment, which is internally terminated with  $50\Omega$  to VCCO<sub>-</sub> - 2V, take the following steps:

- 1) Remove resistors R2 and R27.
- 2) Short resistors R1 and R19.
- 3) Place a bias-T in series between the MAX9601 and the test equipment. Connect the bias-T's RF and DC terminals to the QA output and the RF terminal to the test equipment's PECL input. Then connect the DC terminal to a VCCO<sub>-</sub> - 2V termination voltage through a  $50\Omega$  resistor.

## Layout

The EV kit uses a two-layer board for simplicity. However, special layout precautions have been taken due to the large gain-bandwidth characteristics of the MAX9601. The  $0.01\mu\text{F}$  power-supply decoupling capacitors are mounted as close as possible to the power-supply input pins. The inductance of the return path is reduced by flooding the ground plane with multiple vias. Multiple ground vias are also present besides the decoupling capacitors and signal traces to shorten the ground return path and maximize isolation. The lead lengths on the inputs and outputs are minimized to avoid unwanted parasitic feedback around the comparators. Microstrip layout and terminations are used at both the inputs, as well as the outputs, to reduce signal reflections. Layer 2 is a continuous ground plane with no signal or power traces. Impedance discontinuities have been minimized by routing all the signal traces on the top layer only, with no interconnecting vias or sharp corners. Edge-mount SMA connectors are used to reduce the capacitive discontinuity and maximize frequency response. The symmetric layout also minimizes the skew due to the traces.

## Test Setup

Note that a test setup optimized for high-speed measurement is essential to observe the true performance of the MAX9601 device. Use matched SMA cables for the differential inputs and outputs. Also, account for the time delay and skew of the test setup. For accurate measurement of the device's rise and fall times, an oscilloscope with a bandwidth several times larger than the maximum signal frequency must be used.

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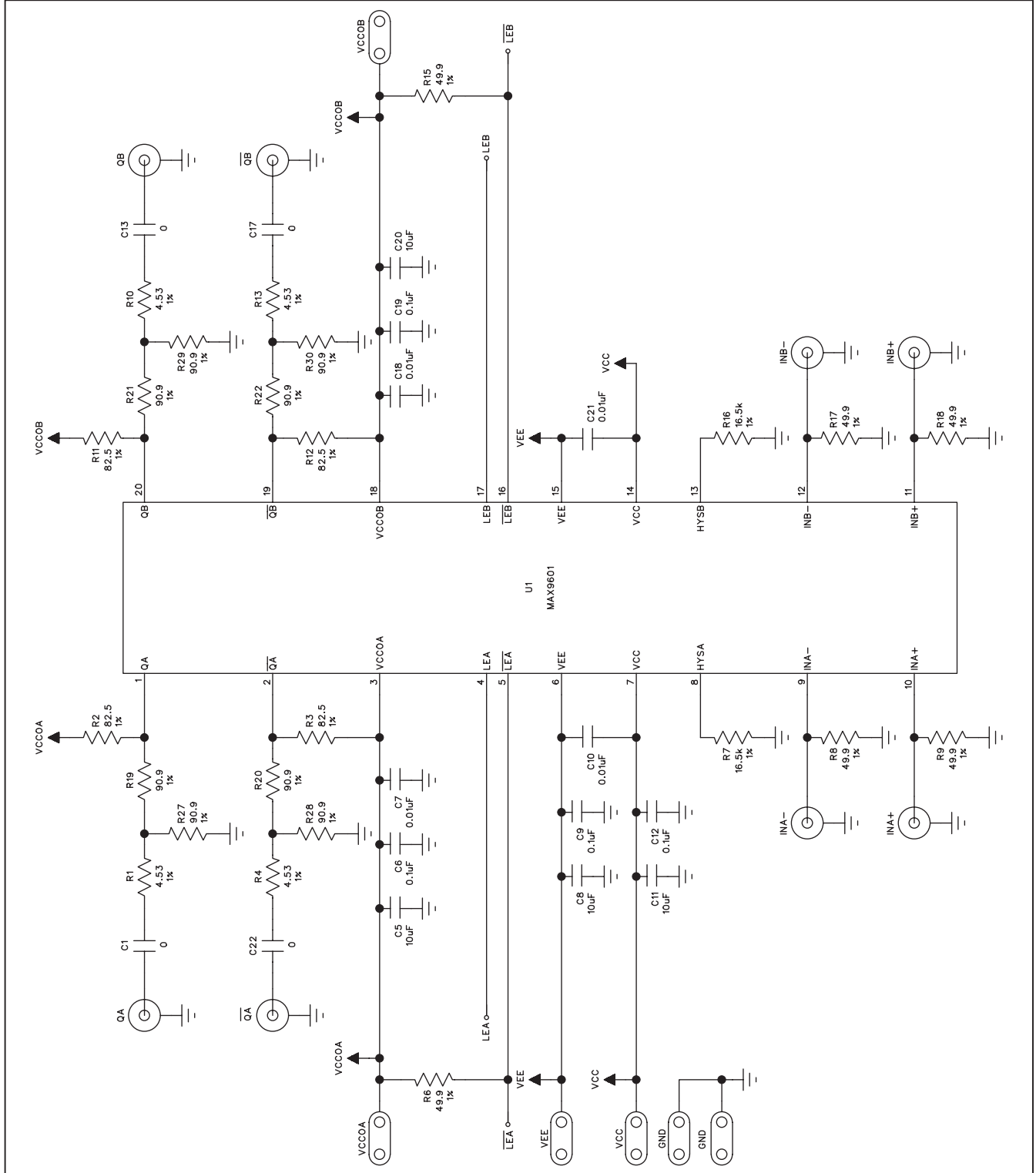


Figure 1. MAX9601 EV Kit Schematic

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Evaluates: MAX9601

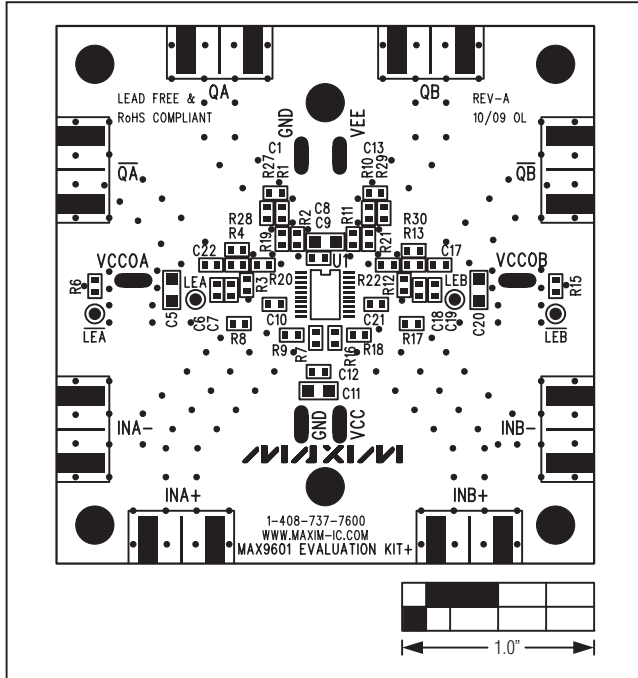


Figure 2. MAX9601 EV Kit Component Placement Guide—Component Side

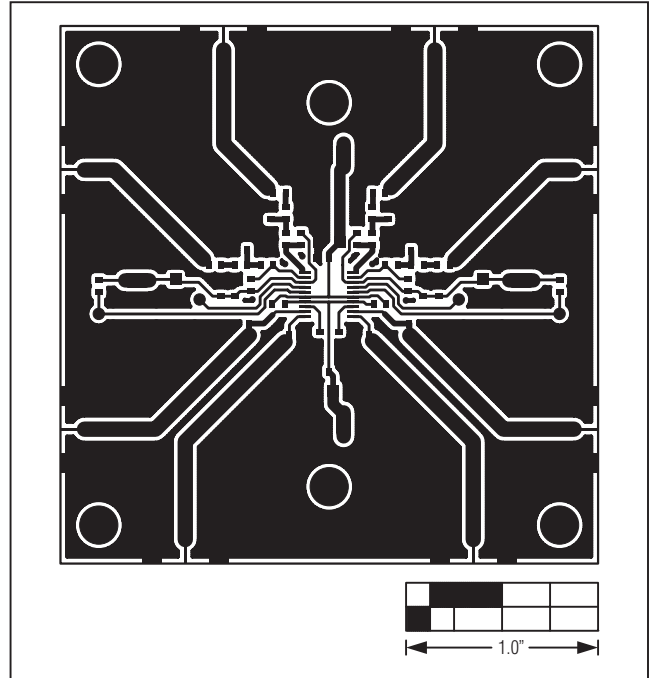


Figure 3. MAX9601 EV Kit Component PCB Layout—Component Side

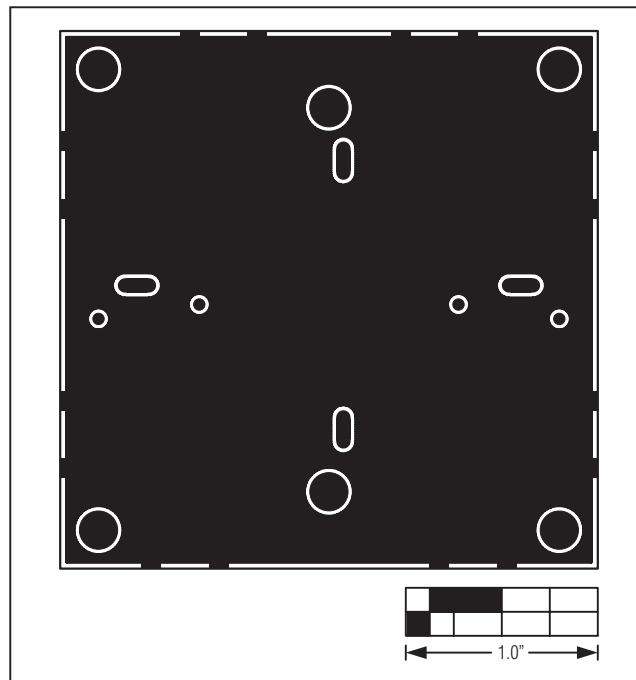


Figure 4. MAX9601 EV Kit PCB Layout—Solder Side

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