AN2681
Application note

ST2S06A33 / ST2S06B
synchronous dual buck converter with reset

Introduction

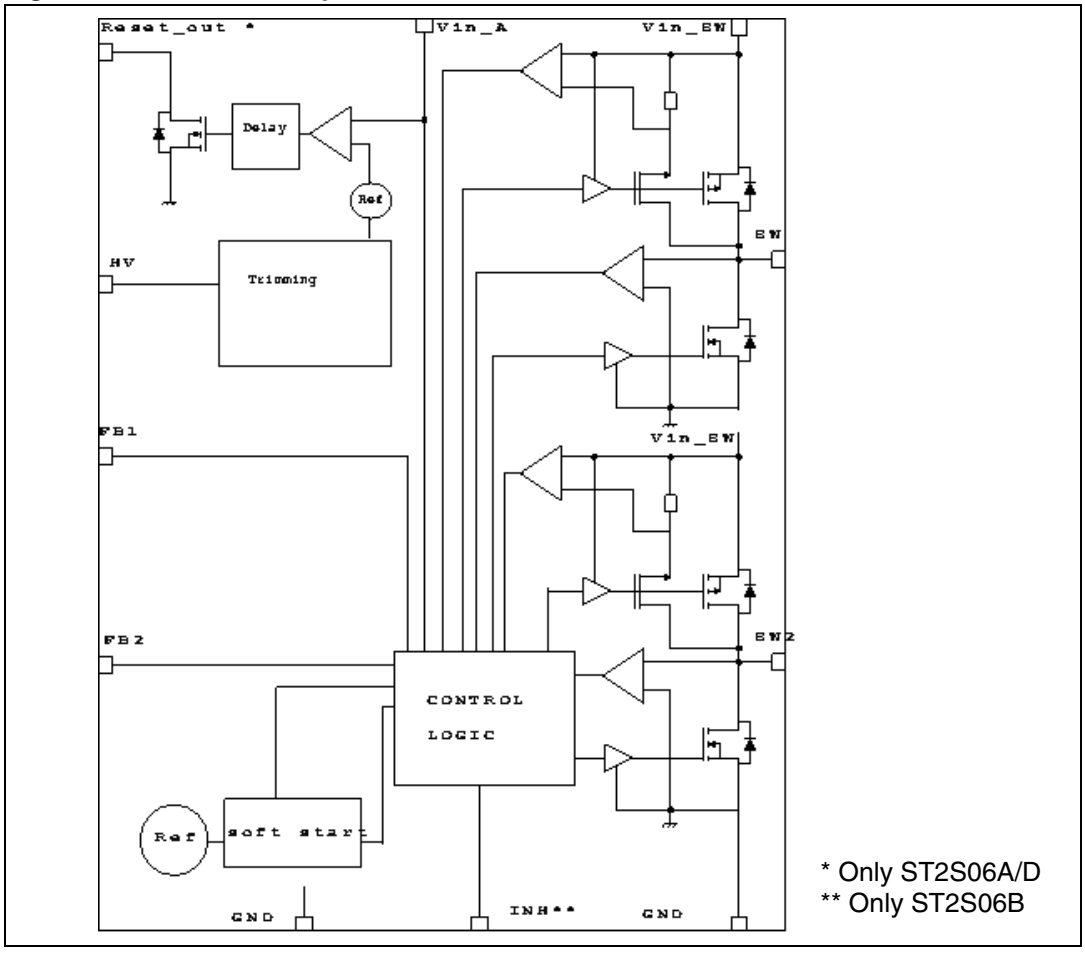
The ST2S06 is a dual synchronous step-down DC-DC converter optimized for powering low-voltage digital cores in ODD applications and, generally, used to replace the high current linear solution when the power dissipation may cause a high heating of the application environment. It provides up to 0.5 A over an input voltage range of 2.5 V to 5.5 V.

A high switching frequency (1.5 MHz) allows the use of tiny surface-mount components. A resistor divider to set the output voltage value, an inductor and two capacitors are required for every channel. In addition, a low output ripple is guaranteed by the current mode PWM topology and by the use of low ESR surface-mount ceramic capacitors.

The device is thermal protected and current limited to prevent damage due to accidental short-circuit.

The family is available in the QFN12L (4x4 mm) package.

Figure 1. ST2S06 - simplified schematic



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1 ST2S06 description

The ST2S06 is a dual adjustable current mode PWM synchronous step-down DC/DC converter with an internal 0.5 A power switch. It is a complete 0.5 A dual switching regulator with internal compensation that eliminates the need for additional components.

The device is available in three versions, the ST2S06A and ST2S06D with a reset function and the ST2S06B with an inhibit function.

The ST2S06 family operates with typically 1.5 MHz fixed frequency.

To maintain good efficiency at both channels, the devices operate in power-save mode at light load (*Figure 2* and *3*). When the load increases it automatically switches to PWM (pulse width modulation) mode in order to reduce the output voltage ripple (*Figure 4* and *5*).

Figure 2. Inductor current at light load

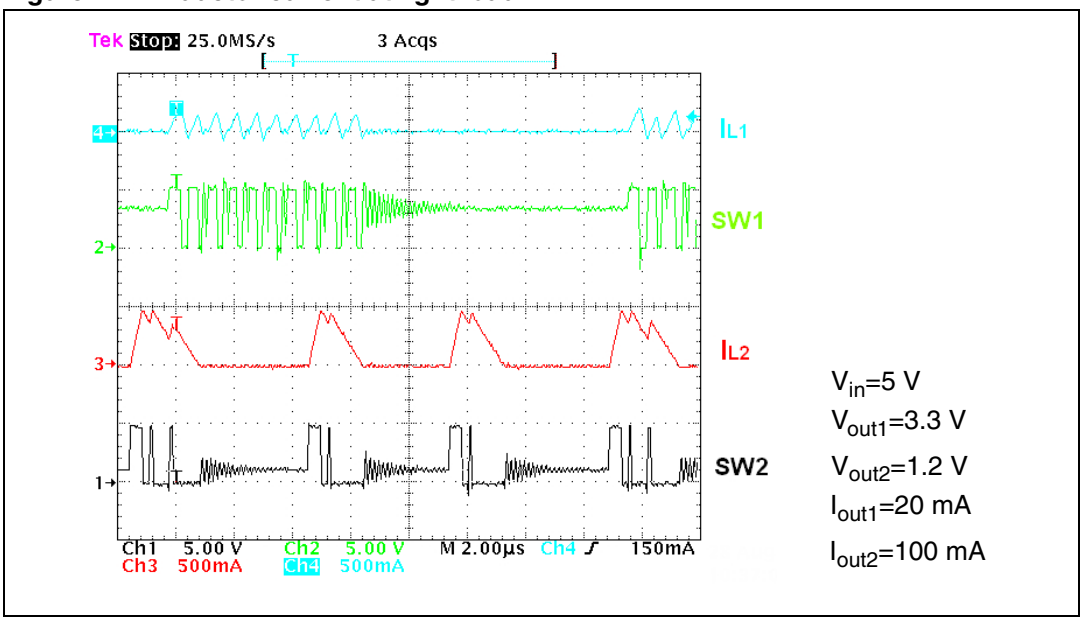


Figure 3. Output voltage ripple at light load

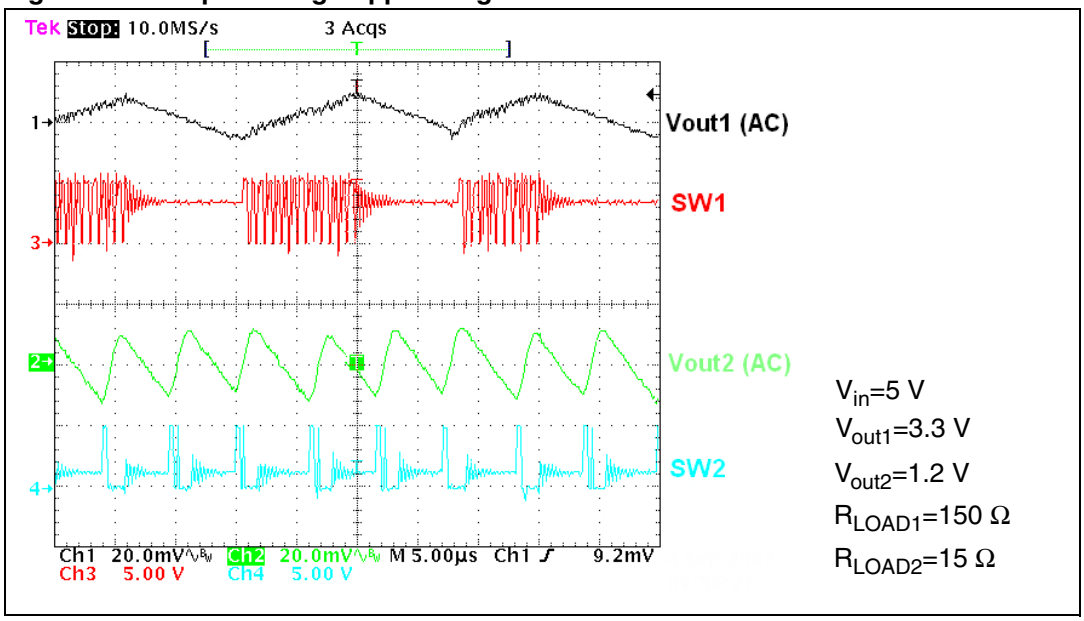


Figure 4. Inductor current in PWM

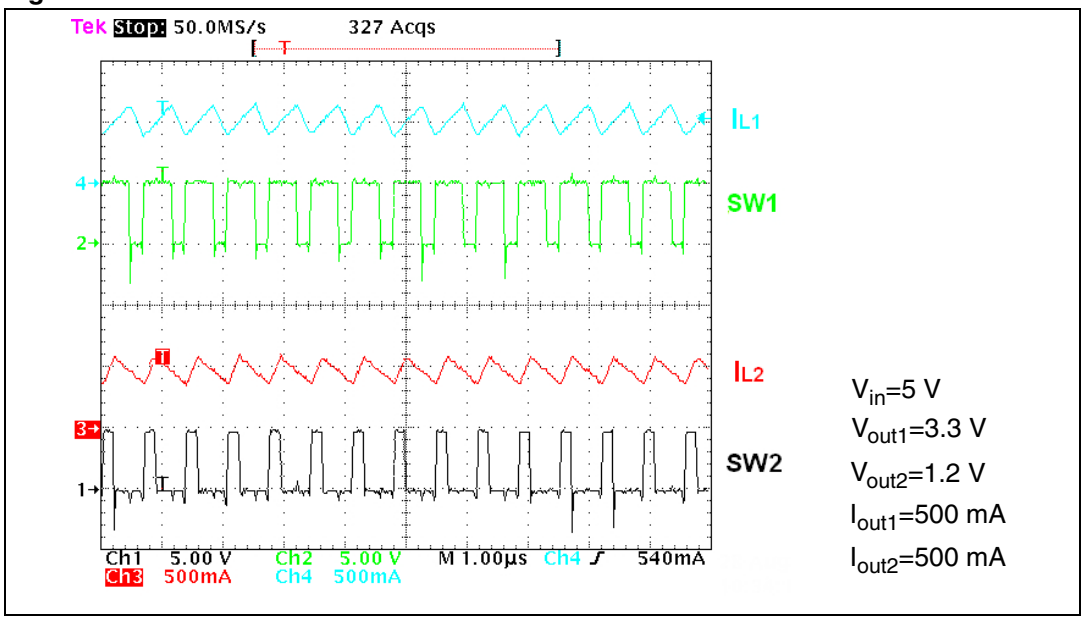
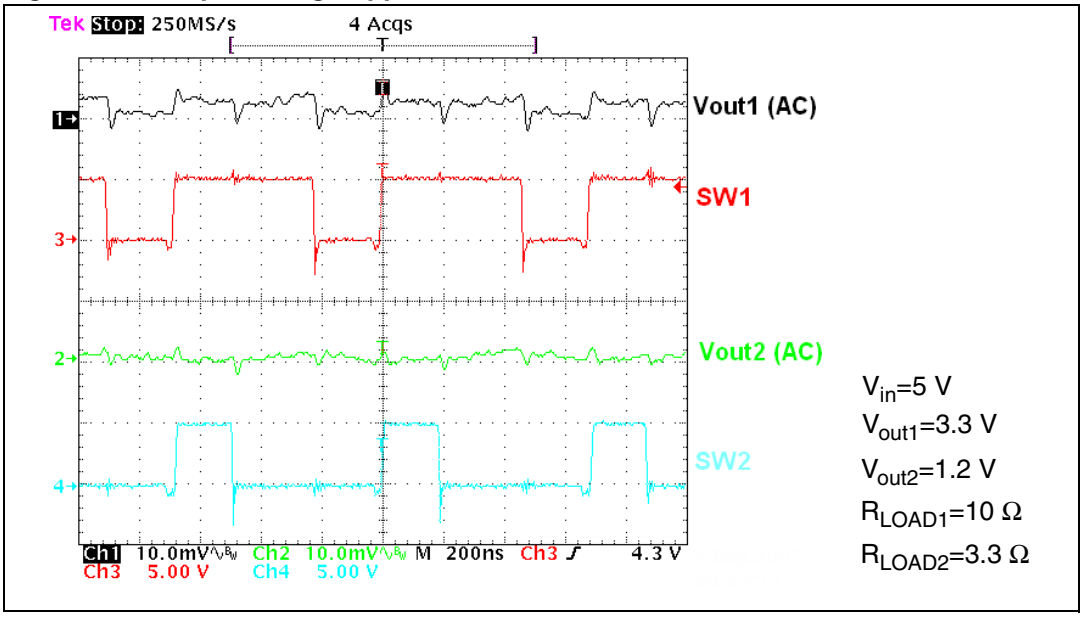
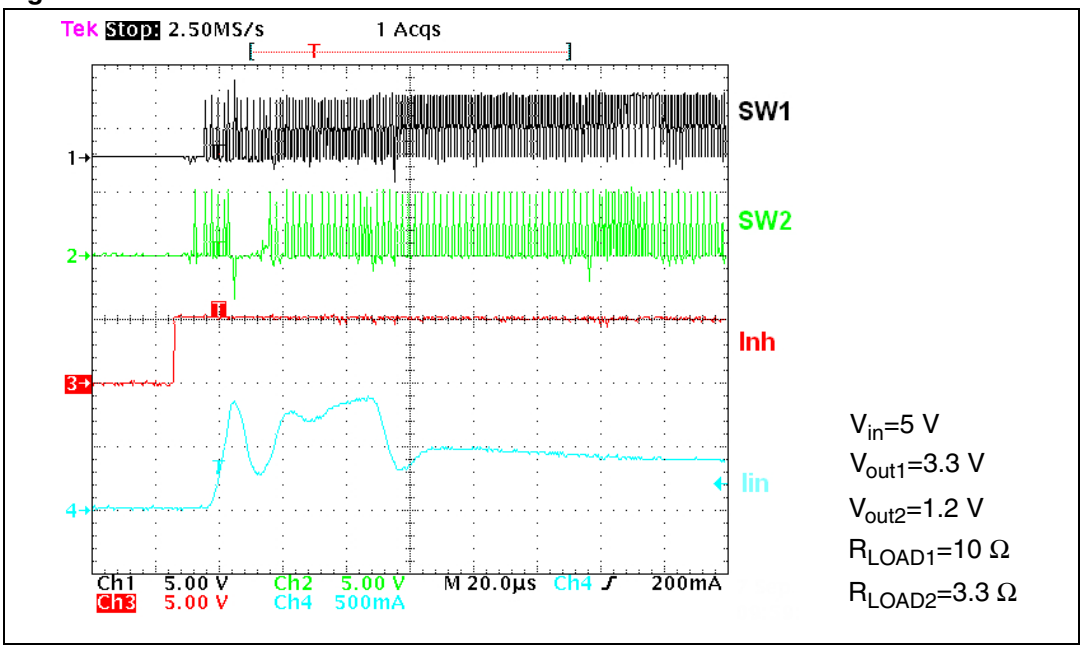


Figure 5. Output voltage ripple in PWM



To clamp the error amplifier reference voltage, a Soft Start control block generating a voltage ramp is implemented. When switching on the power supply, it allows controlling the inrush current value.

Figure 6. Inrush current



Other protection circuits in the device are the thermal shutdown block which turns off the regulator when the junction temperature exceeds 150 °C (typ.) and the cycle-by-cycle current limiting that provides protection against shorted outputs.

Operation of the device requires few components: two inductors, three capacitors and two resistor dividers. The inductors chosen must be capable of not saturating at the peak current level. The value of the inductors should be selected keeping in mind that a large inductor value increases the efficiency at low output current and reduces output voltage ripple, while

a smaller inductor can be chosen when it is important to reduce the package size and the total application cost.

Finally, the ST2S06 family has been designed to work properly with X5R or X7R SMD ceramic capacitors both at input and at output. These capacitors, thanks to their very low series resistance (ESR), minimize the output voltage ripple. Other low ESR capacitors can be used according to the need of the application without compromising the correct functioning of the device.

Due to the high switching frequency and peak current, it is important to optimize the application environment by reducing the length of the PCB traces and placing all external components near the device.

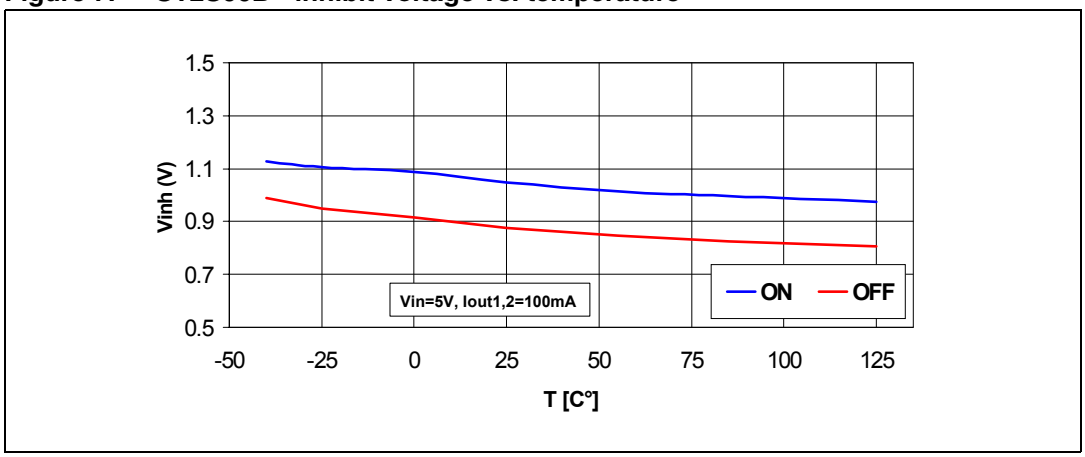
1.1 Inhibit function (ST2S06B only)

The ST2S06B features an Inhibit function (pin 10). When the Inh voltage is higher than 1.3 V the device is On and if it is lower than 0.4 V the device is OFF. In shutdown mode consumption is lower than 1 µA.

The Inh pin does not have an internal pull-up which means that you cannot leave the inhibit floating.

If the inhibit function is not used, the Inh pin must be connected to V_{in}.

Figure 7. ST2S06B - inhibit voltage vs. temperature



1.2 Reset function (ST2S06A and ST2S06D only)

Most ODD applications require a flag showing that the input voltage is in the correct range.

Figure 8. ST2S06A\D - reset block diagram

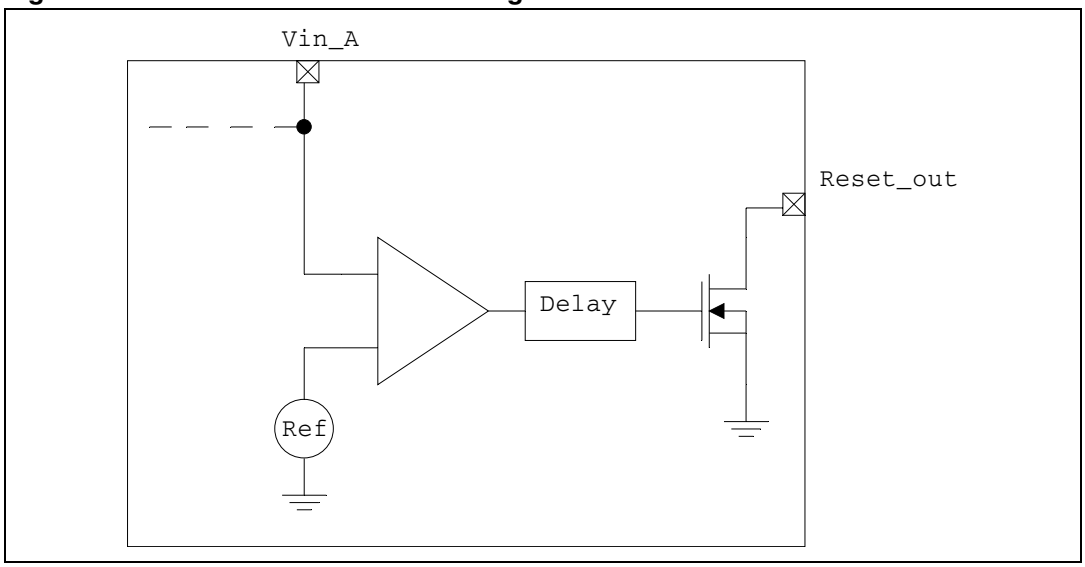
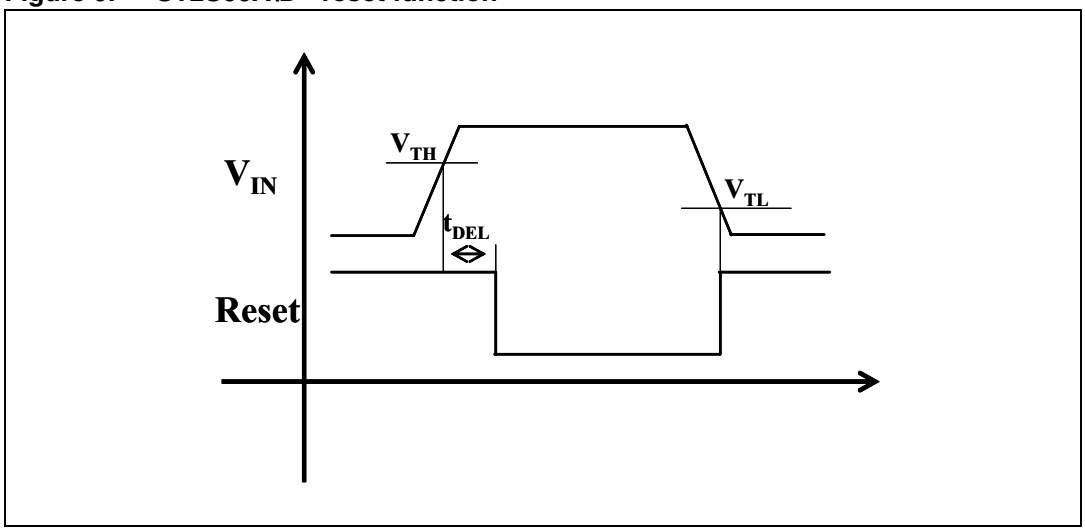


Figure 8 shows the simplified reset block diagram. A comparator senses the input voltage. When it is higher than VTL (4.2 V for ST2S06A or 3.7 V for ST2S06D), the reset_out pin goes to high impedance. If it is below VTH (4.6 V for ST2S06A or 4.55 V max for ST2S06D), the reset_out pin goes to low impedance with a delay of 100 ms (typ.) for ST2S06A or 65 ms (typ.) for ST2S06D (see *Figure 9* and *11*).

Figure 9. ST2S06A\D - reset function



The use of the Reset function requires an external pull-up resistor which must be connected between reset_out pin and V_{in} or V_{out}. We suggest using a pull-up resistor for reset in the range of 100 kΩ to 1 MΩ. If the reset function is not used, the reset_out pin must remain floating on the board.

In the application board (*Figure 10*), Rpi is used to pull up the reset_out pin to V_{in} and Rpo to pull up the reset_out pin to V_{out1}. Of course the reset_out pin can be connected only to V_{in} or V_{out}.

Figure 10. Pull-up resistor

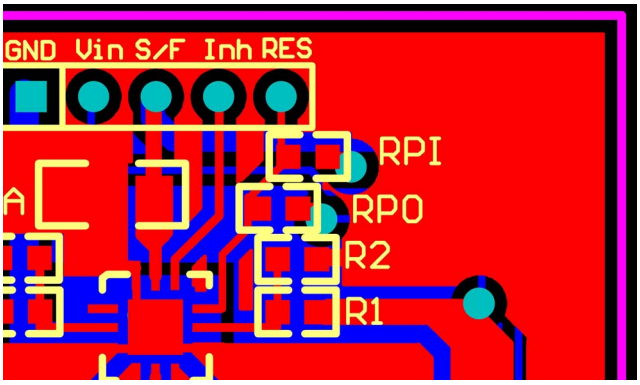


Figure 11. ST2S06D - delay time

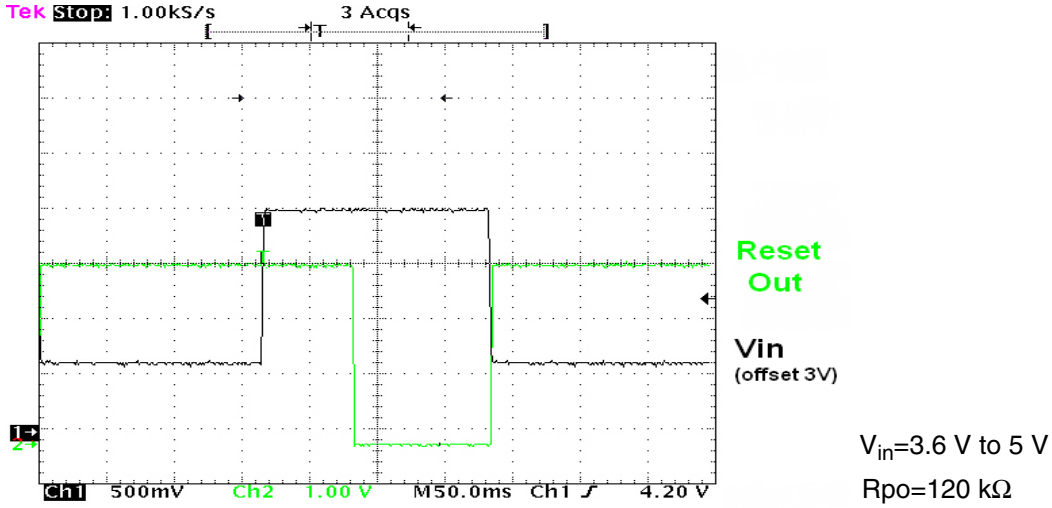


Figure 12. Reset_in threshold vs. temperature

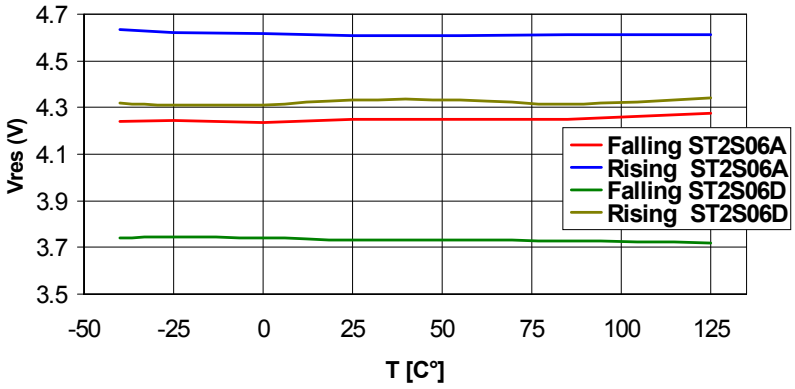
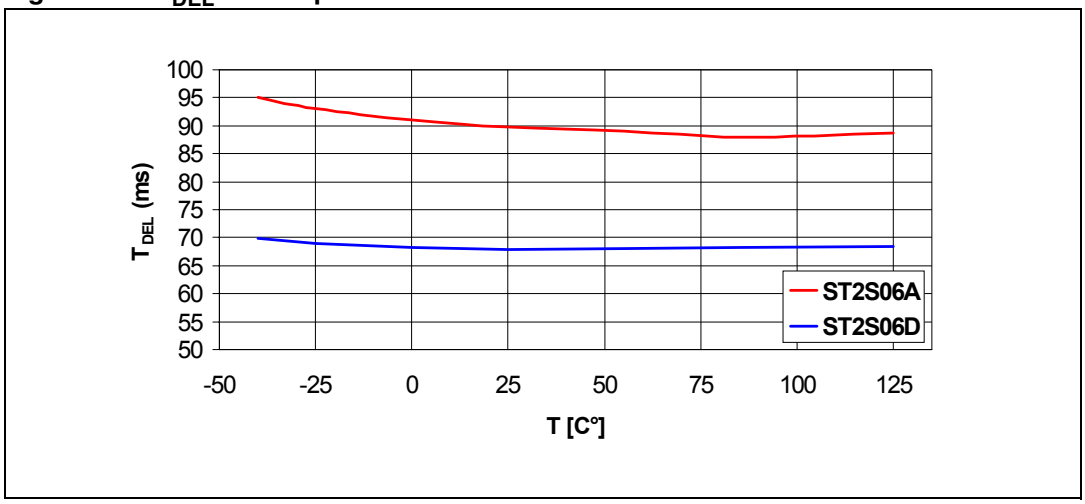


Figure 13. T_{DEL} vs. temperature



1.3 Short-circuit protection

In overcurrent protection mode, when the peak current reaches the current limit, the device reduces T_{on} to its minimum value. In these conditions, the duty cycle is strongly reduced and, in most of the applications, this is enough to limit the current to I_{lim}.

In case of heavy short-circuit at the output (V_{out}=0 V) and depending on the application conditions (V_{in} value and parasitic effect of external components), the current peak could reach values higher than I_{lim}. This can be understood considering the inductor current ripple during the ON and OFF phases:

Equation 1

$$\text{ON phase} \qquad \Delta I_L = \frac{(V_{in} - V_{out} - DCR_L \cdot I)}{L} \cdot T_{on}$$

Equation 2

$$\text{OFF phase} \qquad \Delta I_L = \frac{(V_D + V_{out} + DCR_L \cdot I)}{L} \cdot T_{off}$$

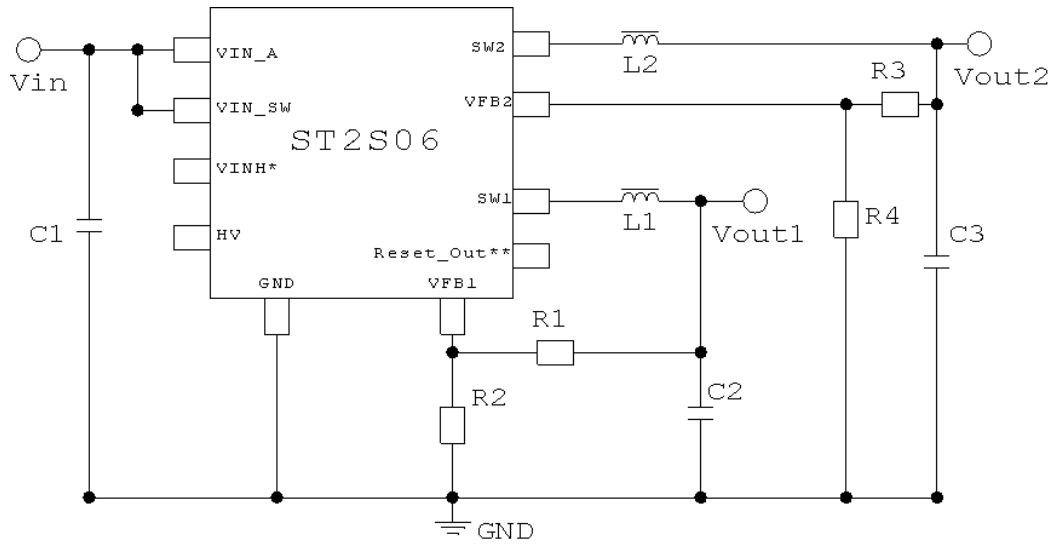
Where V_D is the voltage drop across the internal NMOS and DCR_L is the series resistance of the inductor. In short-circuit conditions V_{out} is negligible. So, during T_{off}, the voltage applied to the inductor is very small and it can be that the current ripple in this phase does not compensate for the current ripple during T_{on}. The maximum current peak can be easily measured through the inductor with V_{out} = 0 V (short-circuit) and V_{in}=V_{inmax}. In case the application has to sustain the short-circuit condition for a long time, the external components (mainly inductor) must be selected based on this value.

2 Selecting components for applications

This section provides information to assist in the selection of the most appropriate components for your applications.

Figure 14 shows the typical application schematic.

Figure 14. Typical application schematic



* ST2S06B
** ST2S06A/D

2.1 Output voltage selection

The output voltage can be adjusted from 0.8 V up to 85% of input voltage value by connecting a resistor divider between the output and the V_{FB} pin.

You must choose the resistor divider according to the following equation:

Equation 3

$$V_{out} = V_{FB}\left[1 + \frac{R_1}{R_2}\right] \quad \text{with } V_{FB}=0.8\ V$$

Figure 13 shows the feedback voltage versus temperature.

We suggest using a resistor with a value in the range of 10 kΩ to 50 kΩ. Lower values are suitable as well, but will increase current consumption. Be aware that the duty cycle must be kept below 85% at all application conditions, so that:

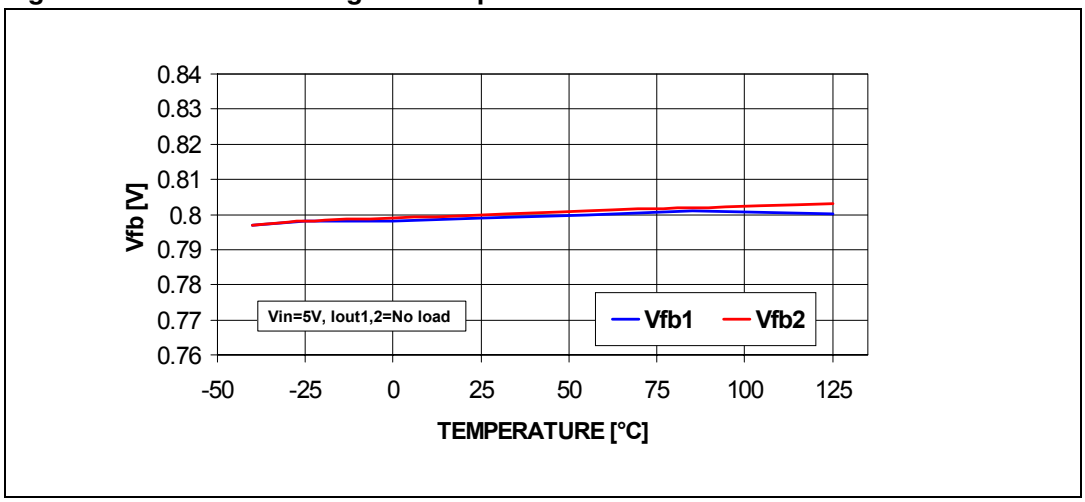
Equation 4

$$D_{MAX} = \frac{V_{out} + V_F}{V_{inMIN} - V_{SW}} < 0.85$$

where V_F is the voltage drop across the internal NMOS, and V_{SW} represents the voltage drop across the internal PMOS.

For output voltages close to the feedback voltage, we suggest adding a very small capacitor in parallel to R1 in the range of 10 pF. Or, as an alternative, we suggest increasing the current in the resistor divider by decreasing the R1 and R2 value.

Figure 15. Feedback voltage vs. temperature



2.2 Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input impulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb all this switching current that can be up to one half of the load current (worst case, with duty cycle of 50%).

For this reason, the quality of these capacitors has to be very high to minimize its power dissipation generated by the internal ESR, thus improving the system reliability and efficiency.

The critical parameter is usually the RMS current rating, which must be higher than the RMS input current. The maximum RMS input current (flowing through the input capacitor) is:

Equation 5

$$I_{RMS} = I_{out} \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta}}$$

Where η is the expected system efficiency, D is the duty cycle, and I_{out} the output DC current. This function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to I_{out} divided by 2 (considering $\eta = 1$).

The maximum and minimum duty cycles are:

Equation 6

$$D_{MAX} = \frac{V_{out} + V_F}{V_{inMIN} - V_{SW}}$$

Equation 7

$$D_{MIN} = \frac{V_{out} + V_F}{V_{inMAX} - V_{SW}}$$

Where V_F it is the voltage drop across the internal NMOS and V_{SW} the voltage drop across the internal PMOS. Considering the range D_{MIN} to D_{MAX} it is possible to determine the max I_{RMS} flowing through the input capacitor.

The use of ceramic capacitors with voltage ratings in the range of 1.5 times the maximum output voltage is recommended.

2.3 Output capacitor

The output capacitor is very important to satisfy the output voltage ripple requirement. Using a small inductor value is useful to reduce the size of the coil, but increases the current ripple. So, to reduce the output voltage ripple a low ESR capacitor is required. The output voltage ripple (V_{OUT_RIPPLE}), in continuous mode, is:

Equation 8

$$V_{outRIPPLE} = \Delta I \cdot \left(ESR + \frac{1}{8 \cdot C_{out} \cdot F_{SW}} \right)$$

where ΔI is the ripple current and F_{SW} is the switching frequency.

The use of ceramic capacitors with voltage ratings in the range of 1.5 times the maximum output voltage is recommended.

2.4 Inductor

The inductor value is very important because it fixes the ripple current flowing through the output capacitor. The ripple current is usually fixed at 20-40% of I_{out_max}, that is 0.1-0.2 A with I_{out_max} = 0.5 A. The inductor value is approximately obtained by the following formula:

Equation 9

$$L = \frac{V_{in} - V_{out}}{\Delta I} \cdot T_{on}$$

where T_{on} is the ON time of the internal switch, given by D · T. The peak current through the inductor is given by:

Equation 10

$$I_{PK} = I_{out} + \frac{\Delta I}{2}$$

And it can be seen that if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. So, for fixed peak current protection, a higher value of the inductor permits a higher value for the output current.

2.5 Layout considerations

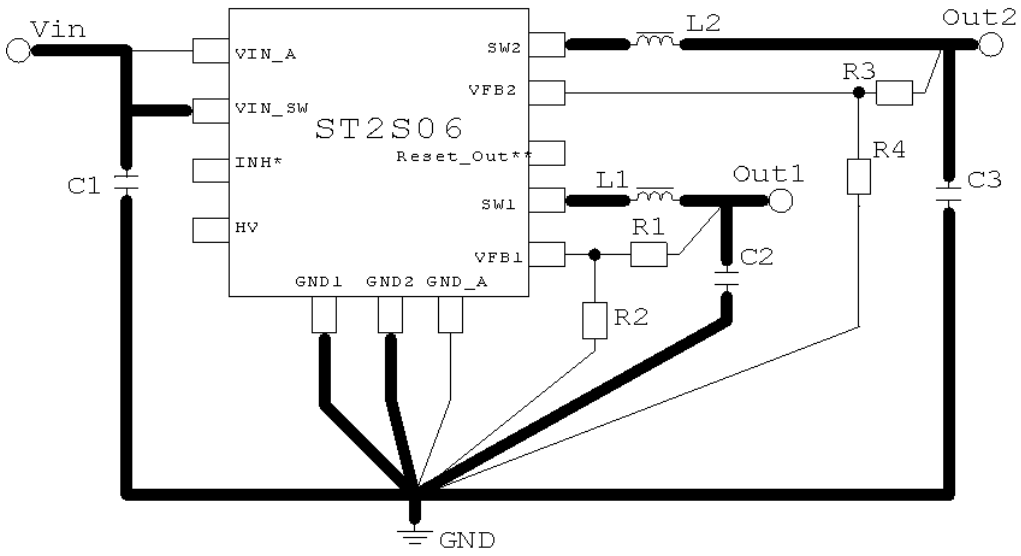
Due to the high switching frequency and peak current, the layout is an important design step for all switching power supplies. If the layout is not carefully done, important parameters such as efficiency and output voltage ripple could be compromised.

Short, wide traces must be implemented for main current and for power ground paths as shown in bold in *Figure 16*. The input capacitors must be placed as close as possible to the device pins as well as the inductors and output capacitors.

A common ground node minimizes ground noise, as shown in *Figure 16*.

HV pin must be floating or connected to GND and the exposed pad of the package must be connected to GND.

Figure 16. Layout considerations



* ST2S06B
** ST2S06A/D

3 Thermal considerations

The dissipated power of the device is determined by three different factors:

- Switch losses due to the nonnegligible $R_{DS(on)}$. These are equal to:

Equation 11

$$P_{ONP} = R_{DS(on)P} \cdot I^2_{out} \cdot D$$

and

Equation 12

$$P_{ONN} = R_{DS(on)N} \cdot I^2_{out} \cdot (1-D)$$

where D is the duty cycle of the application.

Note: The duty cycle is theoretically given by the ratio between V_{out} and V_{in}, but in practice is quite higher than this value in order to compensate the losses of the overall application. Due to this reason, the switch losses related to the $R_{DS(on)}$ increase compared to the ideal case.

- On and Off switching losses. These are given by the following relationship:

Equation 13

$$P_{SW} = V_{in} \cdot I_{out} \cdot \frac{(T_{on} + T_{off})}{2} \cdot F_{SW} = V_{in} \cdot I_{out} \cdot T_{SW} \cdot F_{SW}$$

where T_{ON} and T_{OFF} are the overlap times of the voltage across the power switch and the current flowing into it during the turn-on and turn-off phases. TSW is the equivalent switching time.

- Quiescent current losses:

Equation 14

$$P_Q = V_{in} \cdot I_Q$$

where I_Q is the quiescent current.

The overall losses are:

Equation 15

For channel 1

$$P_{CH1} = R_{DS(on)P1} \cdot I^2_{out1} \cdot D_1 + R_{DS(on)N1} \cdot I^2_{out1} \cdot (1 - D_1) + V_{in} \cdot I_{out1} \cdot T_{SW1} \cdot F_{SW1}$$

Equation 16

For channel 2

$$P_{CH2} = R_{DS(on)P2} \cdot I^2_{out2} \cdot D_2 + R_{DS(on)N2} \cdot I^2_{out2} \cdot (1 - D_2) + V_{in} \cdot I_{out2} \cdot T_{SW2} \cdot F_{SW2}$$

Equation 17

$$P_{TOT} = P_{CH1} + P_{CH2} + V_{in} \cdot I_Q$$

The junction temperature of device is:

Equation 18

$$T_J = T_A + Rth_{J-A} \cdot P_{TOT}$$

where T_A is the ambient temperature and Rth_{J-A} is the thermal resistance junction to ambient.

4 Demonstration board usage recommendation

The demonstration board shown in *Figure 17* is provided with a Kelvin connection which means that for each pin there are two lines available, one used to supply or sink current and the other one used to perform the needed measurement.

Figure 17. Demonstration board layout

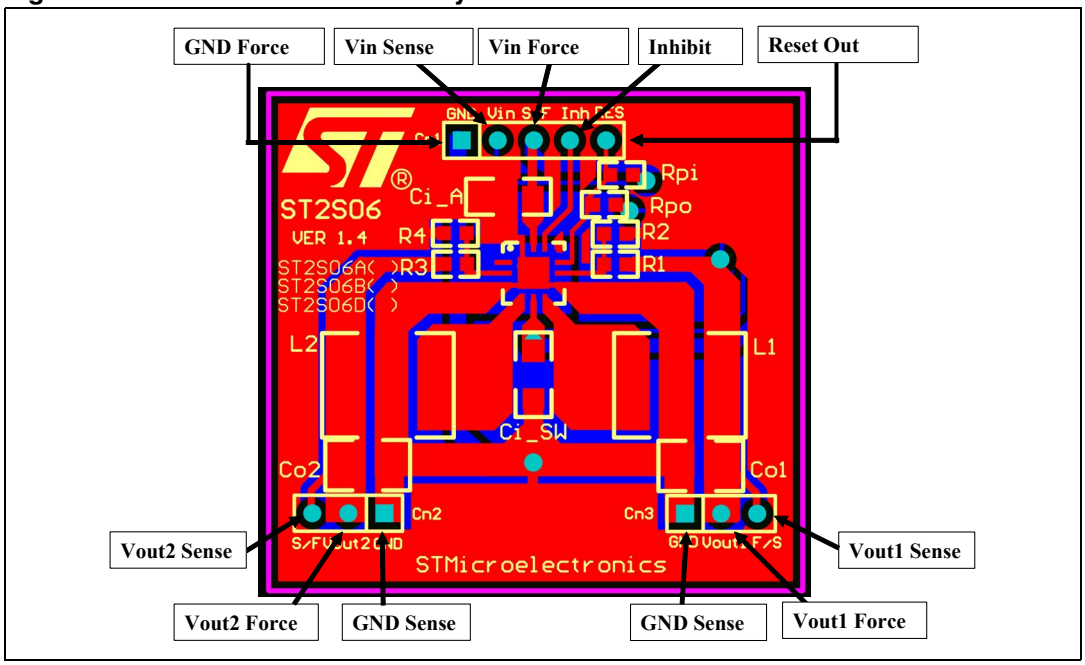


Figure 18. Demonstration board - top layer

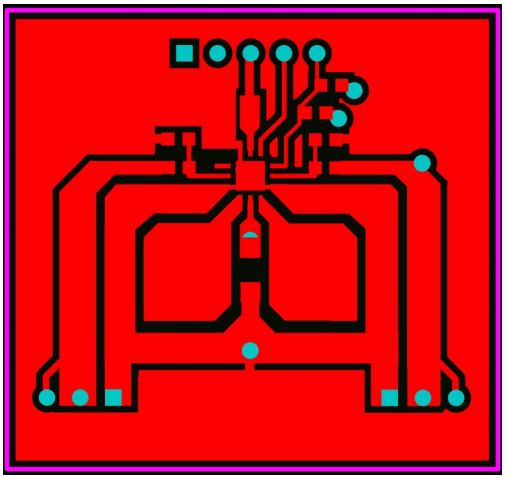
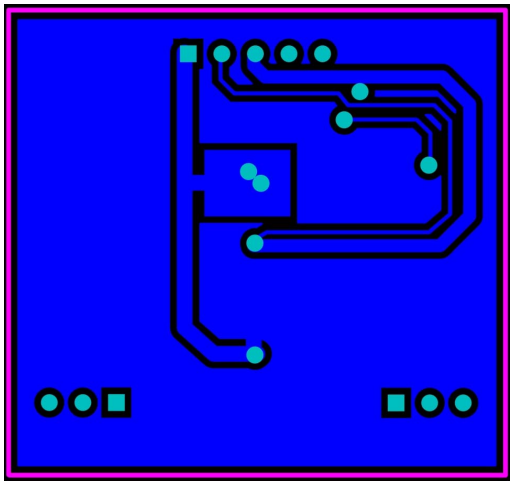


Figure 19. Demonstration board - bottom layer



The board has one inhibit pin available which is located on the top side of the board. This pin can be used to supply the inhibit pin with an external voltage higher than 1.3 V to turn on, or lower than 0.4 V to turn off the device.

4.1 External component selection

Figure 19 and *20* show the demonstration board schematic.

Figure 20. Demonstration board schematic for ST2S06A\D

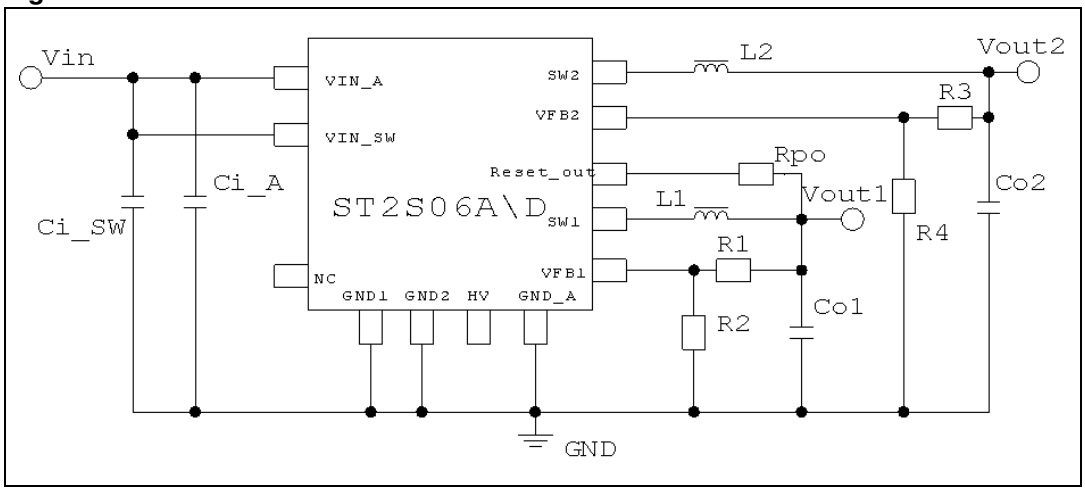
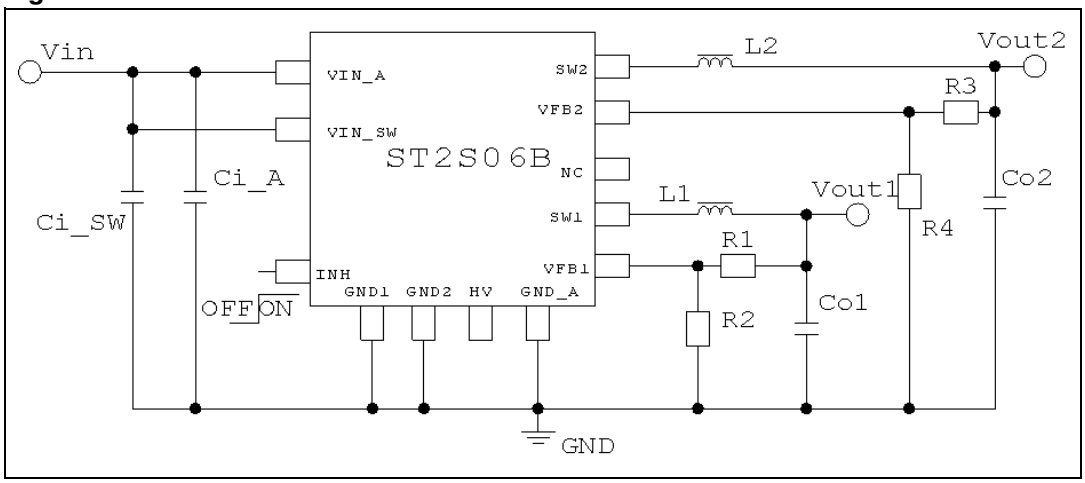


Figure 21. Demonstration board schematic for ST2S06B



In order to obtain the needed output voltage, the resistor divider must be selected in accordance with the following formula:

Equation 19

$$V_{OUT1,2} = V_{FB1,2}\left[1 + \frac{R_{1,3}}{R_{2,4}}\right]$$

with $V_{FB1,2} = 0.8$ V

Table 1. Recommended resistor divider

$V_{OUT1,2}$	$R_{1,3}$	$R_{2,4}$
1.2 V	27 kΩ	47 kΩ
3.3 V	47 kΩ	15 kΩ

The resistors dividers in *Table 1* are a good compromise in terms of current consumption and minimum output voltage.

Note: If ST2S06A33 or ST2S06D33 are mounted in the demonstration board, R1 is replaced with a short-circuit and R2 is not used.

4.1.1 Capacitors selection

It is possible to use any X5R or X7R ceramic capacitor

- Ci_A = Ci_SW = 4.7 µF (ceramic) or higher.
- Co1 = Co2 = 22 µF (ceramic) or higher. It is possible to put several capacitors in parallel in order to reduce the equivalent series resistance and improve the ripple present in the output voltage.

4.1.2 Inductor selection

Due to the high frequency (1.5 MHz) it is possible to use very small inductors values. In our board the device was tested with inductors in the range of 1 µH to 10 µH, with very good efficiency performances (see below plot in *Figure 22*).

As the device is able to provide an operative output current of 0.5 A, the use of inductors capable of managing at least 1.5 A is strongly recommended.

Figure 22. Efficiency vs. output current

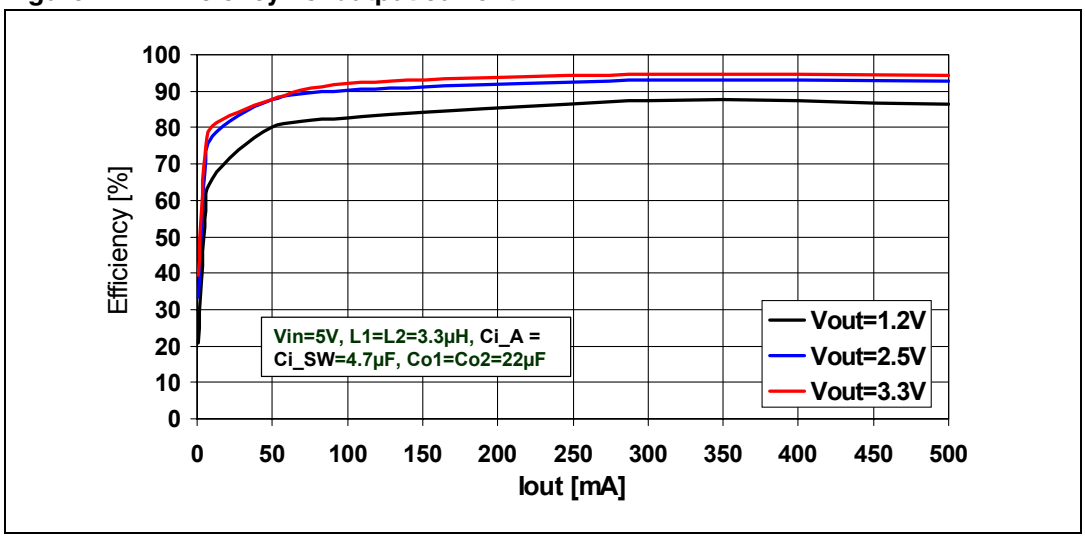


Figure 23. Efficiency vs. inductor

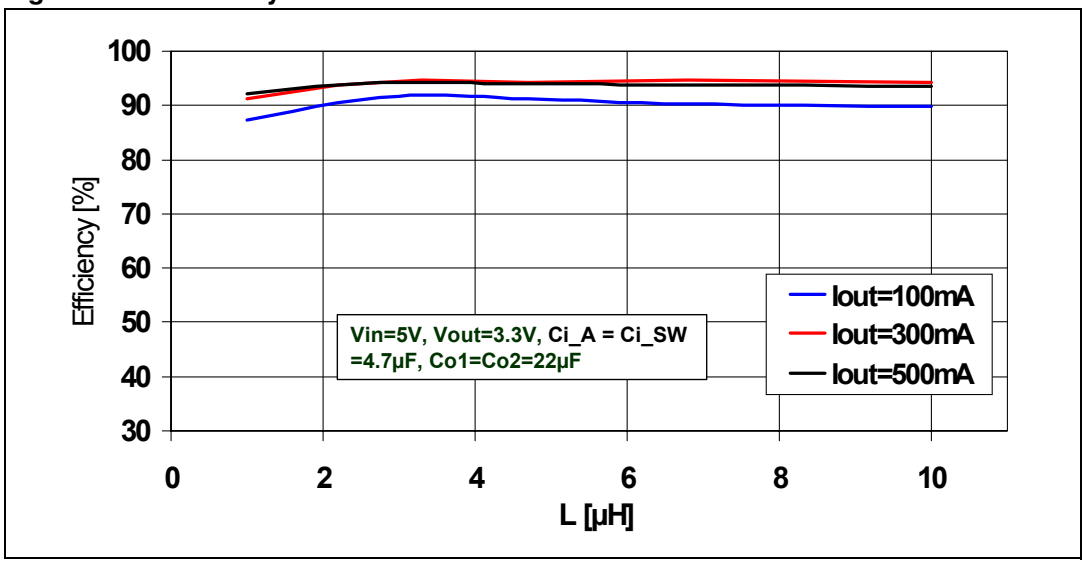
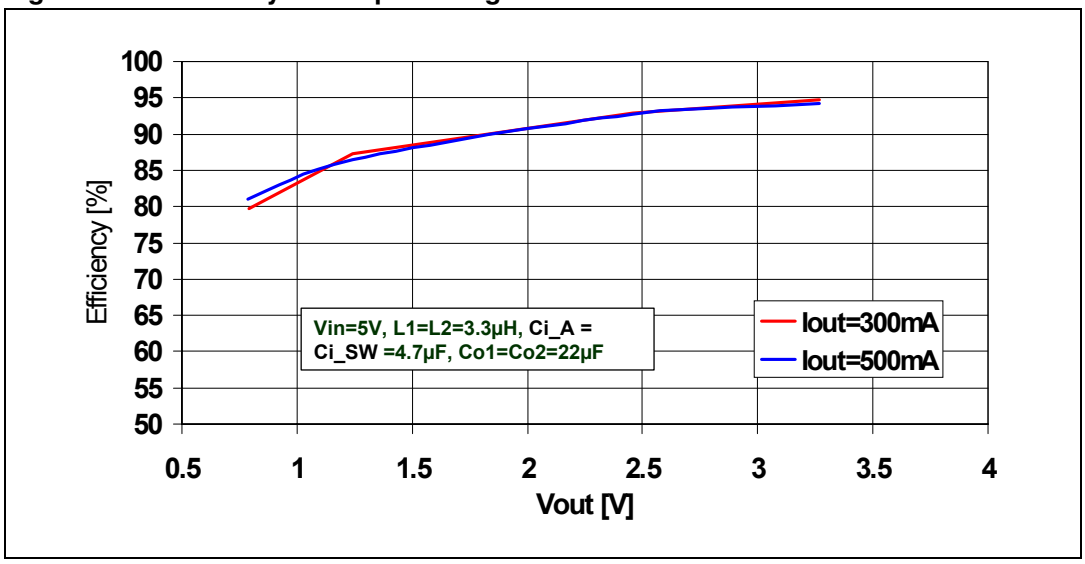


Figure 24. Efficiency vs. output voltage



Note: All efficiencies are relative to one channel, the other channel is at no-load.

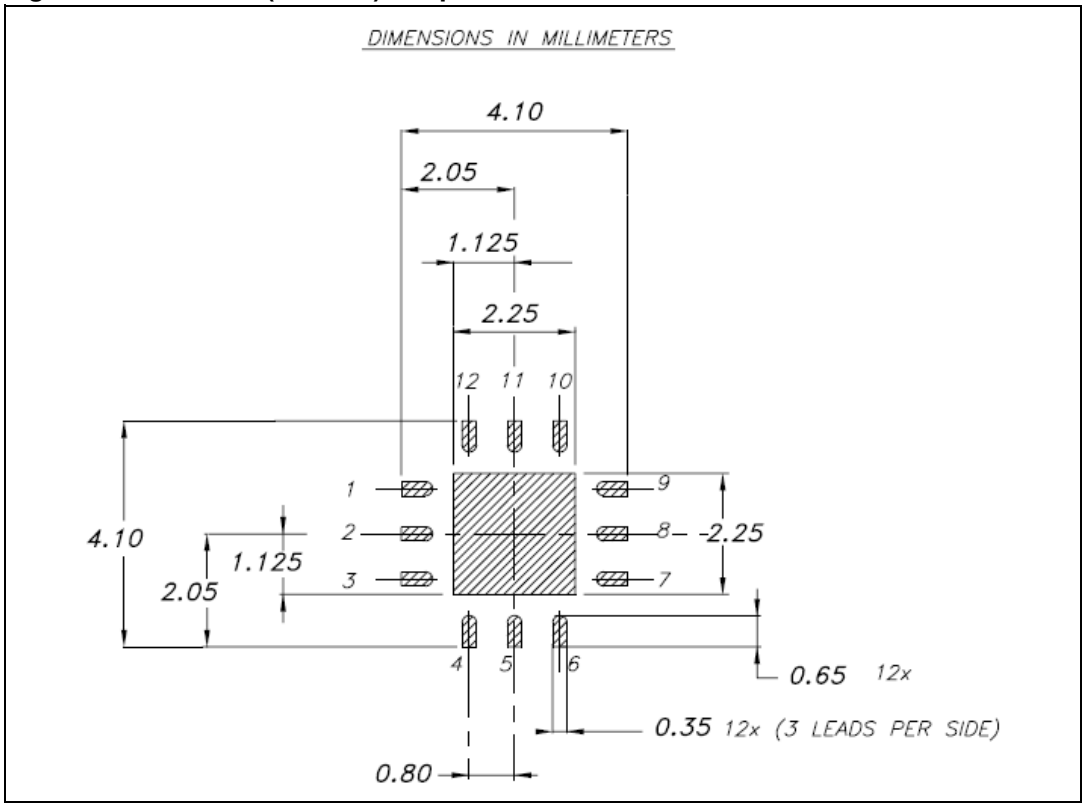
5 Bill of materials

Table 2. BOM with most common components

Name	Value	Material	Manufacturer	P/N
Ci_A	4.7 µF	Ceramic	Murata	GRM21BR61E475KA12B
		Ceramic	TDK	C3216X7R1C475K
Ci_SW	4.7 µF	Ceramic	Murata	GRM21BR61E475KA12B
		Ceramic	TDK	C3216X7R1C475K
Co1	22 µF	Ceramic	Murata	GRM32ER61E226KE15B
		Ceramic	TDK	C3225X7R1C226M
Co2	22 µF	Ceramic	Murata	GRM32ER61E226KE15B
		Ceramic	TDK	C3225X7R1C226M
L1	3.3 µH		TDK	RLF7030T-3R3M4R1
			Murata	LQH66SN3R3M03L
			Coiltronics	DR73-3R3
L2	3.3 µH		TDK	RLF7030T-3R3M4R1
			Murata	LQH66SN3R3M03L
			Coiltronics	DR73-3R3
Rpi/Rpo	120 kΩ			

6 Recommended footprint

Figure 25. QFN12L (4x4 mm) footprint recommended data



7 Revision history

Table 3. Document revision history

Date	Revision	Changes
08-Jan-2008	1	Initial release
15-Sep-2008	2	Changed: *Figure 22*, *24*