Structure Silicon Monolithic Integrated Circuit
Product Power Management LSI for Multimedia LSI on Cellular

Type **BH6173GUL**

Functions
- 1ch 500mA, high efficiency Step-down Converter. (16 steps adjustable Vout by I^2C)
- 3-channel CMOS-type LDOs. (16 steps adjustable Vout by I^2C)
- LDO and Stepdown converter Power ON/OFF control enabled by I2C interface
- I^2C compatible Interface. (Selectable device address is "1001010"and "1001111")
- Wafer Level CSP package(2.05mm × 2.05mm) for space-constrained applications.

Absolute Maximum Ratings(Ta=25℃)

Parameter	Symbol	Rating	Unit
Maximum Supply Voltage (VBAT1,PVCC, PBAT)	VBATMAX	6.0	V
Maximum Supply Voltage (VIO)	VIOMAX	4.5	V
Maximum Input Voltage 1 (LX, FB, OUT1, OUT2, OUT3, ADRS)	VINMAX1	VBAT + 0.3	V
Maximum Input Voltage 2 (NRST, CLK, DATA)	VINMAX2	VIO + 0.3	V
Power Dissipation	Pd	690*[1]	mW
Operating Temperature Range	Topr	-35 ～ +85	℃
Storage Temperature Range	Tstg	-55 ～ +125	℃

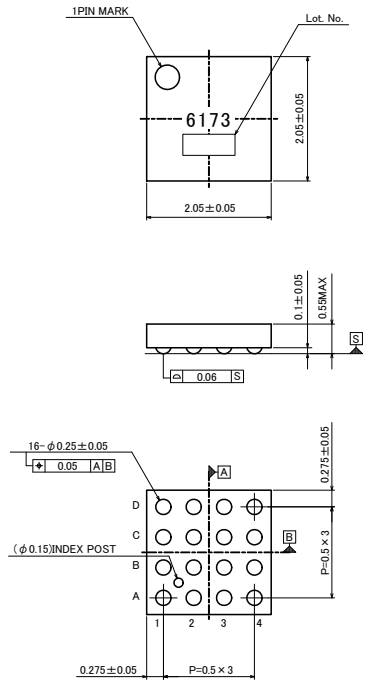
*1 This is the allowable loss of when it is mounted on a ROHM specification board 50mm×58mm.
To use at temperature higher than 25℃ , derate 1% per 1℃.

Recommended Operating Conditions (Ta=25℃)

Parameter	Symbol	Range	Unit
VBAT, PBAT Voltage	VBAT	*[2] 2.20 ～ 5.20	V
VIO Voltage	VIO	*[3] 1.70 ～ 4.20	V

*2 Whenever the VBAT, PVCC and PBAT voltage is under the LDO, SWREG output voltage, the LDO and SWREG output is not guaranteed to meet its published specifications.
*3 The VIO Voltage must be under the Battery Voltage VBAT, PBAT at any times.
*This product is not especially designed to be protected from radioactivity.

● Overview Dimensions (VCSP50L2)

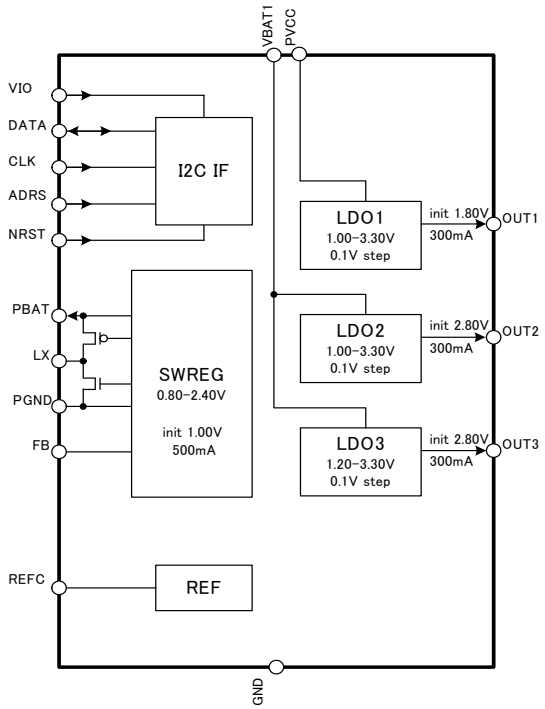


Unit (mm)

● Ball Descriptions

Ball No.	PIN Name
B2	DATA
C3	CLK
D3	VBAT1
D1	PVCC
A1	PBAT
A2	LX
A3	PGND
A4	FB
C2	NRST
C1	OUT1
D2	OUT2
D4	OUT3
C4	REFC
B1	VIO
B4	GND
B3	ADRS

● Block Diagram



Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PVCC=PBAT=3.6V, VIO=2.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
●Circuit Current						
VBAT Circuit Current 1 (OFF)	IQ1	-	0.4	1	μA	LDO1~3=OFF, SWREG1=OFF, NRST=L, VIO=0V
Circuit Current 2 (Standby)	IQ2	-	0.7	1.4	μA	LDO1~3=OFF, SWREG1=OFF, NRST=H, VIO=2.6V
Circuit Current 3 (Active)	IQ3	-	170	350	μA	LDO1~3=ON(no load, initial voltage) SWREG1=ON (no load、initial voltage Addres06h="00" PWM/PFM AUTO MODE) NRST=H, VIO=2.6V

Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=PVCC=PBAT=3.6V, VIO=2.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Condition
●Logic pin character							
NRST (CMOS input)	Input high level	VIH1	VIO×0.7	-	VIO+0.3	V	
	Input low level	VIL1	-0.3	-	VIO×0.3	V	
	Logic input current	IIC1	0	0.3	1	μA	Pin Voltage: VIO
ADRS (CMOS input)	Input high level	VIH2	VBAT×0.7	-	VBAT+0.3	V	
	Input low level	VIL2	-0.3	-	VBAT×0.3	V	
	Logic input current	IIC2	-1	0	1	μA	Pin Voltage: VBAT
CLK, DATA (CMOS input)	Input high level	VIH3	VIO×0.8	-	VIO+0.3	V	
	Input low level	VIL3	-0.3	-	VIO×0.2	V	
	Logic input current	IIC3	-1	0	1	μA	Pin Voltage: VIO
DATA (CMOS input)	Output low level	VOL	-	-	0.4	V	I_{OL}=6mA
●SWREG							
SWREG	Output Voltage	VOSW	0.942	1.000	1.058	V	Initial value, Io=100mA
●LDOs							
LDO1	Output voltage	VOM1	1.746	1.800	1.854	V	Initial value Io=1mA
LDO2	Output voltage	VOM2	2.716	2.800	2.884	V	Initial value Io=1mA
LDO3	Output voltage	VOM3	2.716	2.800	2.884	V	Initial value Io=1mA

●Use-related Cautions

(1) Absolute maximum ratings

If applied voltage (VBAT1, VBAT2, PBAT, , VIO), operating temperature range (Topr), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.

(2) Recommended operating range

This is the range within which it is possible to obtain roughly the expected characteristics. For electrical characteristics, it is those that are guaranteed under the conditions for each parameter. Even when these are within the recommended operating range, voltage and temperature characteristics are indicated.

(3) Reverse connection of power supply connector

There is a risk of damaging the LSI by reverse connection of the power supply connector. For protection from reverse connection, take measures such as externally placing a diode between the power supply and the power supply pin of the LSI.

(4) Power supply lines

In the design of the board pattern, make power supply and GND line wiring low impedance.

When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well.

Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.

(5) GND voltage

Make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.

(6) Shorts between pins and misinstallation

When installing in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is installed erroneously, there is a risk of LSI damage. There also is a risk of damage if it is shorted by a foreign substance getting between pins or between a pin and a power supply or GND.

(7) Operation in strong magnetic fields

Be careful when using the LSI in a strong magnetic field, since it may malfunction.

(8) Inspection in set board

When inspecting the LSI in the set board, since there is a risk of stress to the LSI when capacitors are connected to low impedance LSI pins, be sure to discharge for each process. Moreover, when getting it on and off of a jig in the inspection process, always connect it after turning off the power supply, perform the inspection, and remove it after turning off the power supply. Furthermore, as countermeasures against static electricity, use grounding in the assembly process and take appropriate care in transport and storage.

(9) Input pins

Parasitic elements inevitably are formed on an LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.

(10) Ground wiring pattern

When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.

(11) Externally attached capacitors

When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.

(12) Thermal shutdown circuit (TSD)

When the junction temperature reaches the defined value, the thermal shutdown circuit operates and turns the switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(13) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(14) Rush Current

Extra care must be taken on power coupling, power, ground line impedance, and PCB design while excess amount of rush current might instantly flow through the power line when powering-up a LSI which is equipped with several power supplies, depending on on/off sequence, and ramp delays.

Notes

No copying or reproduction of this document, in part or in whole, is permitted without the consent of ROHM Co.,Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing ROHM's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from ROHM upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, ROHM shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM and other parties. ROHM shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While ROHM always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/