

LTC3882-1 ERRATA

The errata below describe conditions that cause an LTC[®]3882-1 device to operate differently than expected or described in the data sheet.

ERRATA SUMMARY

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ERRATA #1: BOOST REFRESH PULSE WIDTH

Boost refresh pulse width cannot readily be programmed to 50ns or 250ns.

Conditions:

This issue occurs at all valid operating conditions.

Impact:

Only two boost refresh pulse widths are readily available: 25ns (the effective factory EEPROM default) and 125ns, according to the following table. The value written to MFR_PWM_MODE_LTC3882-1 is correctly retrieved by a PMBus read of this command.

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MFR_PWM_MODE_LTC3882-1 Supported Values:

BIT	MEANING
7	Output voltage range select: 0: Maximum $V_{OUT} = 5.25V$. 1: Maximum $V_{OUT} = 2.65V$.
6*	Enable V_{OUT} servo.
5	External temperature sense: 0: ΔV_{BE} measurement. 1: Direct voltage measurement.
4:3	BOOST refresh width: 11b: 125ns 10b: 125ns 01b: 25ns 00b: 25ns
2	(Reserved).
1	PWM control protocol: 0: 3-State PWM output. 1: 3-State PWM output with no DCM (including soft-start) or hardware ROC response (including OV).
0	PWM mode: 0: Forced continuous inductor current. 1: Discontinuous inductor current.

*This bit is ignored (servo disabled) if MFR_VOUT_AVP for this channel is programmed to a value greater than 0.0%.

Product Errata

Root Cause:

Internal firmware does not move bit[3] of MFR_PWM_MODE_LTC3882-1 to the proper hardware register. This bit in the hardware register retains its POR value of 0 when MFR_PWM_MODE_LTC3882-1 is written.

Workarounds:

Several workarounds are possible, depending on the system configuration and requirements. Additional workarounds may be possible. Contact LTC Factory Applications for assistance.

Use Continuous Conduction Mode for the Choke – If light load efficiency is not a major concern, simply select Forced Continuous Inductor Current by setting bit[0] in MFR_PWM_MODE_LTC3882-1 to 0. In this mode, the boost refresh pulse width setting is not used. The top-side FET boost supply reservoir capacitor will automatically be refreshed every PWM cycle.

Select an Appropriate Power Stage Design – If DCM operation is desired for light load efficiency, select a power stage design that will allow boost capacitor refresh with a bottom FET ON pulse width of 25ns or 125ns. The selected width should allow the pump capacitor to charge to the minimum VGS required by the top power FET for switching in its SOA, plus one diode drop. The LTC3882-1 will only allow a maximum of eight PWM cycles in DCM without some form of boost refresh.

ERRATA #2: VOUT_TRANSITION_RATE

Actual margin or VOUT_COMMAND transition rates may be inaccurate for very slow voltage changes when the output is in low range.

Conditions:

The following conditions, when present simultaneously, may expose this problem:

- 1) Output range set to low (bit[7] = 1, MFR_PWM_MODE_LTC3882-1).
- 2) VOUT_TRANSITION_RATE set below 10mV/ms.

Impact:

Errors of more than 20% can exist in the time required to transition to the next programmed output voltage. Generally, the error will tend to create a faster transition than programmed.

Root Cause:

An internal firmware constant for handling calculation remainders is incorrect in low range.

Workarounds:

Several workarounds are possible, depending on the system configuration and requirements. Additional workarounds may be possible. Contact LTC Factory Applications for assistance.

Use Higher VOUT Transition Rates – Increasing the programmed value of VOUT_TRANSITION_RATE to 10mV/ms or more will produce reasonably accurate output transitions in both output voltage ranges.

Use High Range for Programming VOUT – Set MFR_PWM_MODE_LTC3882-1 bit[7] to 0 to select high range for programming VOUT. Output transitions will be consistent with the programmed value of VOUT_TRANSITION_RATE over the entire range specified in the datasheet.