RENESAS

Data Sheet

NP35N04YUG

MOS FIELD EFFECT TRANSISTOR

R07DS0016EJ0100
Rev.1.00
Jul 01, 2010

Description

The NP35N04YUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
  — $R_{DS(on)}$ = 10 mΩ MAX. (V_{GS} = 10 V, I_D = 17.5 A)
- Low Ciss: Ciss = 1900 pF TYP. (V_{DS} = 25 V, V_{GS} = 0 V)
- Designed for automotive application and AEC-Q101 qualified
- Small size package 8-pin HSON

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP35N04YUG -E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	8-pin HSON, Taping (E1 type)
NP35N04YUG -E2-AY *1			8-pin HSON, Taping (E2 type)

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±35	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±105	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	77	W
Total Power Dissipation (T_A = 25°C) *2	P_{T2}	1.0	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Repetitive Avalanche Current *3	I_{AR}	22	A
Repetitive Avalanche Energy *3	E_{AR}	48	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.95	°C/W
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	150	°C/W

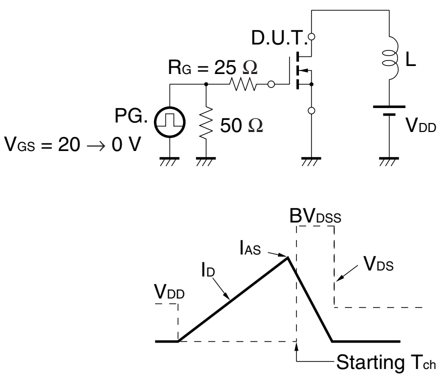
Notes: *1. T_C = 25°C, PW ≤ 10 μs, Duty Cycle ≤ 1%
*2. Mounted on glass epoxy substrate of 40 mm x 40 mm x 0.8 mmt
*3. $T_{ch(peak)}$ ≤ 150°C, R_G = 25 Ω

Electrical Characteristics (T_A = 25°C)

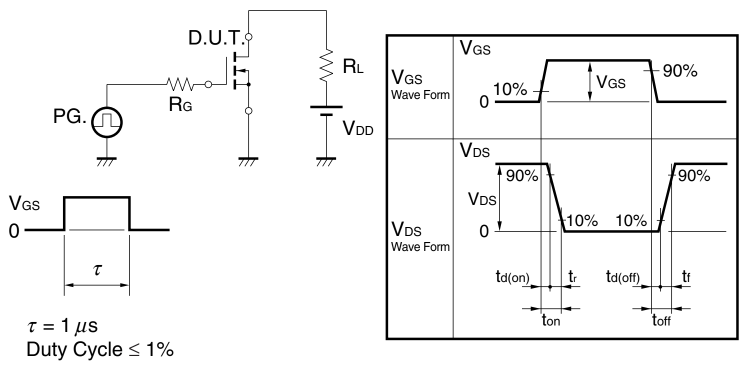
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	V_{DS} = 40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Forward Transfer Admittance *1	$\mid y_{fs} \mid$	8.0	16		S	V_{DS} = 5 V, I_D = 17.5 A
Drain to Source On-state Resistance *1	$R_{DS(on)}$		7.9	10	mΩ	V_{GS} = 10 V, I_D = 17.5 A
Input Capacitance	C_{iss}		1900	2850	pF	V_{DS} = 25 V,
Output Capacitance	C_{oss}		190	290	pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		120	220	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		18	36	ns	V_{DD} = 20 V, I_D = 17.5 A,
Rise Time	t_r		10	25	ns	V_{GS} = 10 V,
Turn-off Delay Time	$t_{d(off)}$		38	76	ns	R_G = 0 Ω
Fall Time	t_f		5	13	ns	
Total Gate Charge	Q_G		36	54	nC	V_{DD} = 32 V,
Gate to Source Charge	Q_{GS}		10		nC	V_{GS} = 10 V,
Gate to Drain Charge	Q_{GD}		12		nC	I_D = 35 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	I_F = 35 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		31		ns	I_F = 35 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		30		nC	di/dt = 100 A/μs

Note: *1. Pulsed

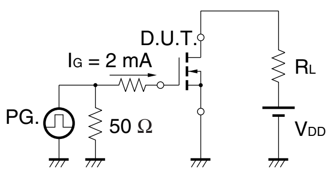
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

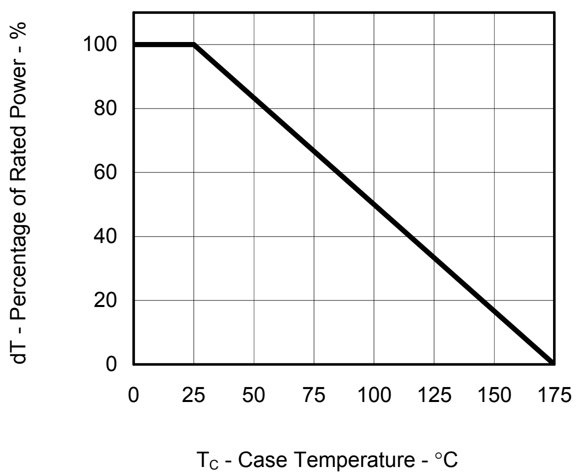


TEST CIRCUIT 3 GATE CHARGE

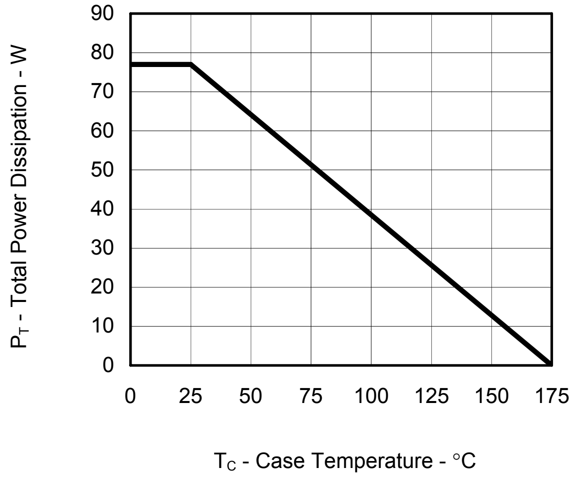


Typical Characteristics (T_A = 25°C)

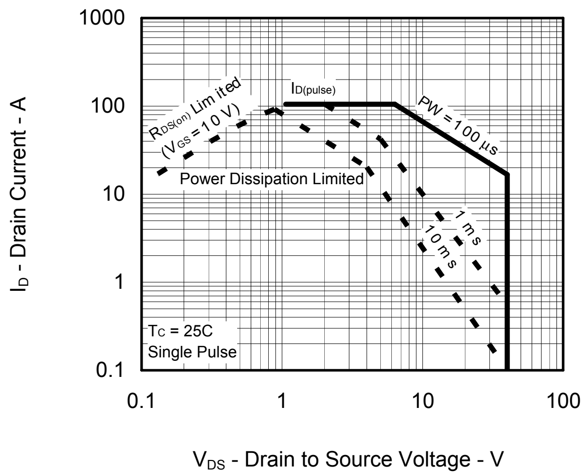
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



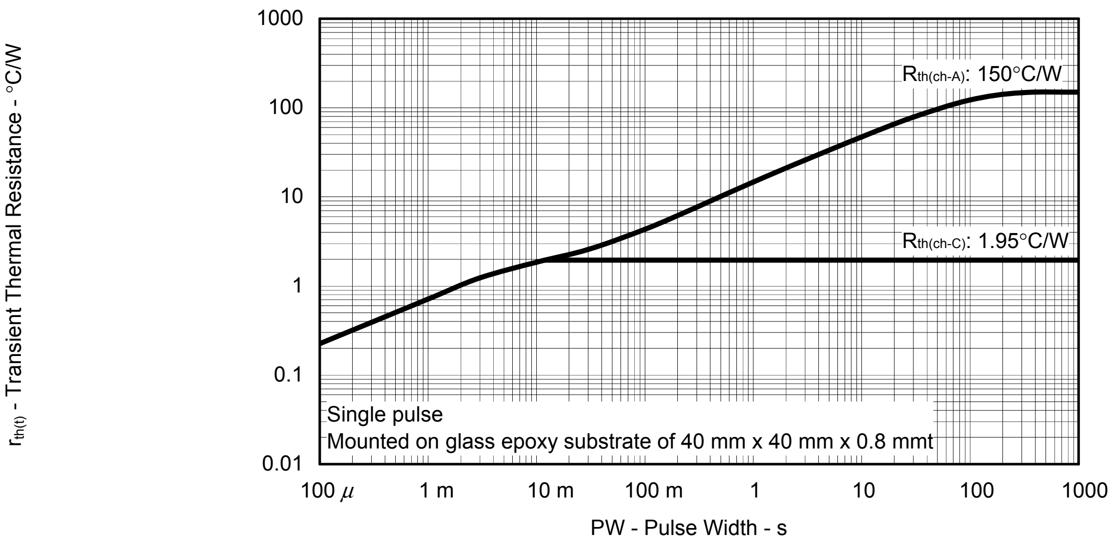
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



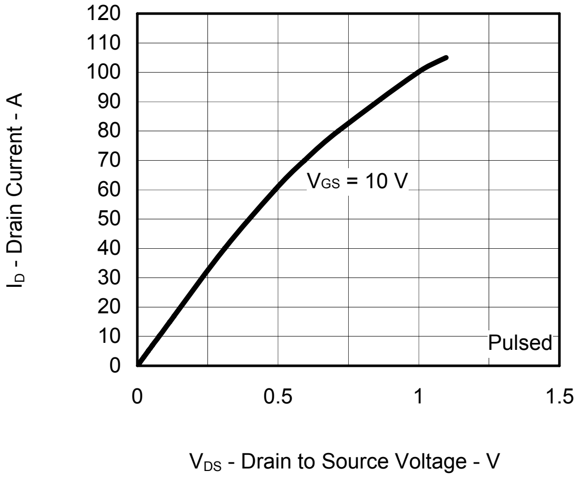
FORWARD BIAS SAFE OPERATING AREA



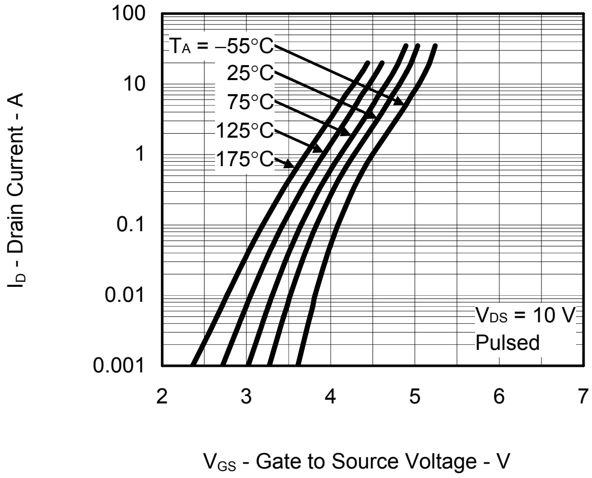
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



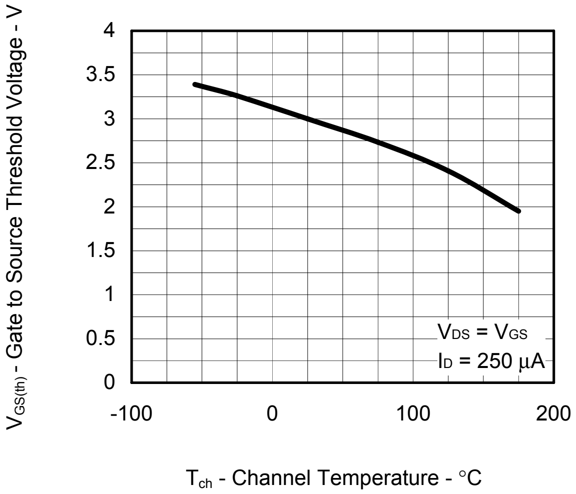
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



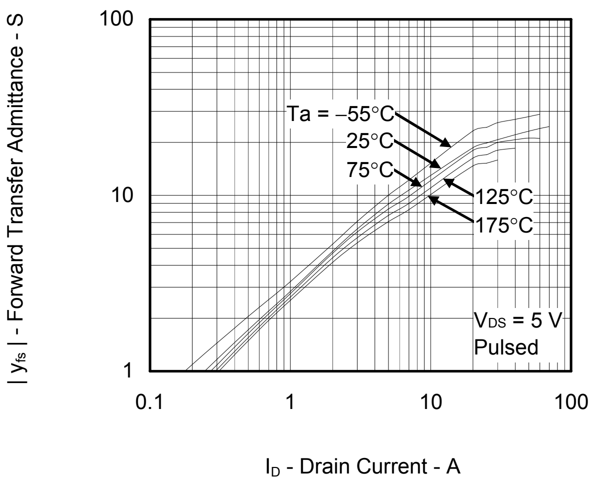
FORWARD TRANSFER CHARACTERISTICS



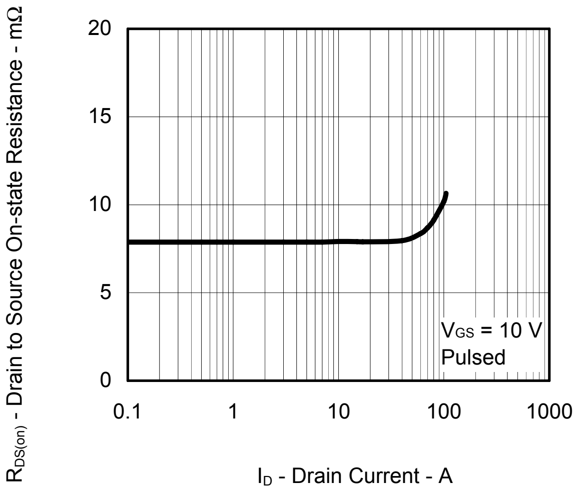
GATE TO SOURCE THRESHOLD VOLTAGE
vs. CHANNEL TEMPERATURE



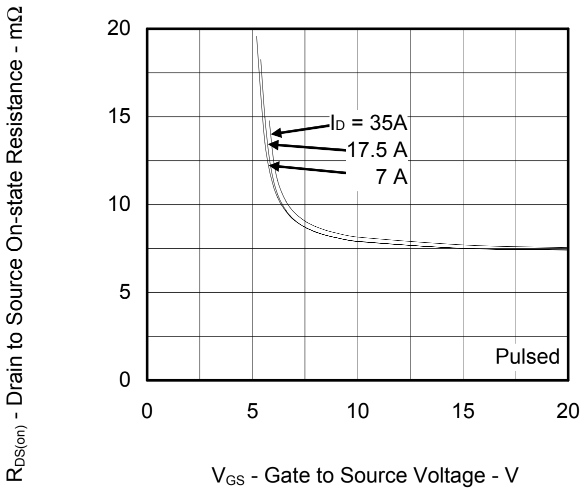
FORWARD TRANSFER ADMITTANCE vs. DRAIN
CURRENT



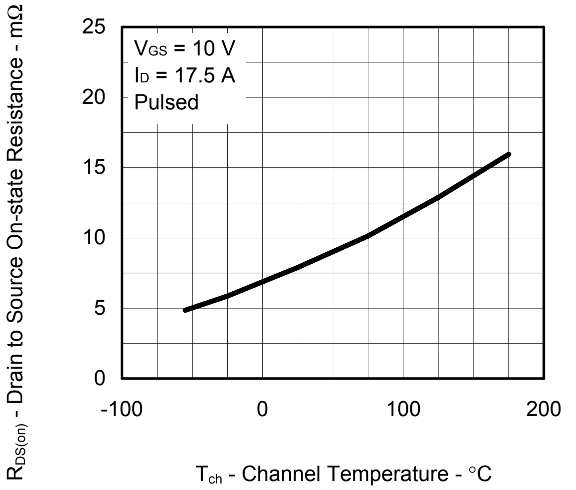
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



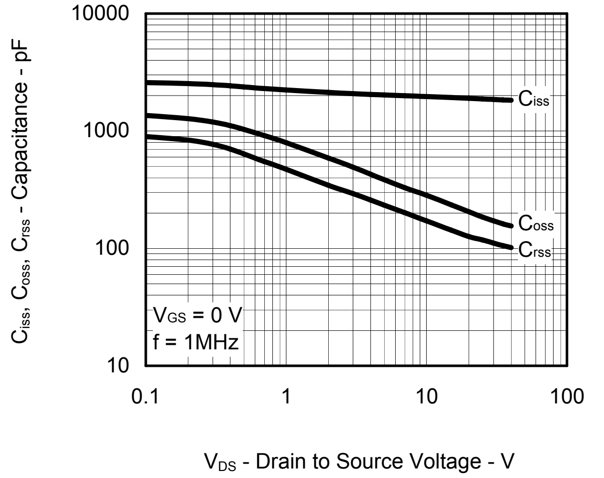
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



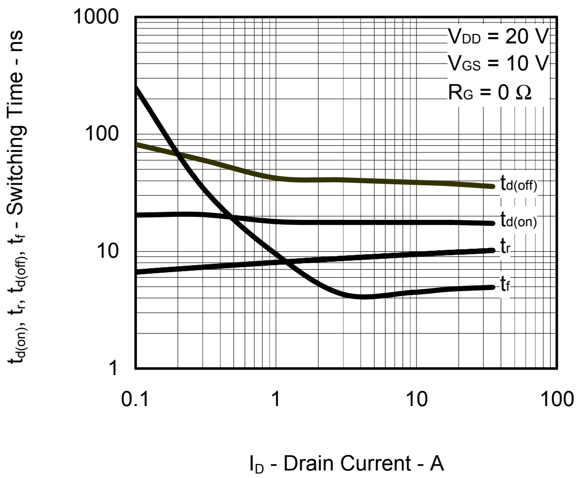
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



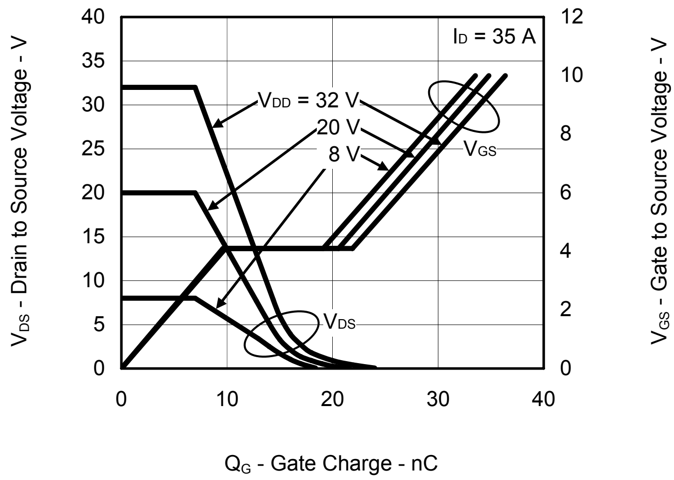
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



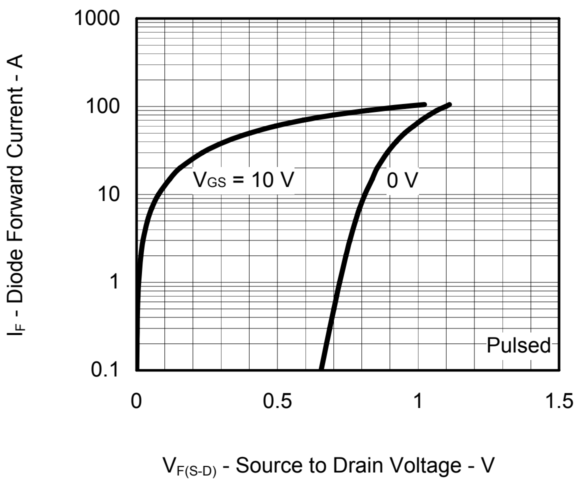
SWITCHING CHARACTERISTICS



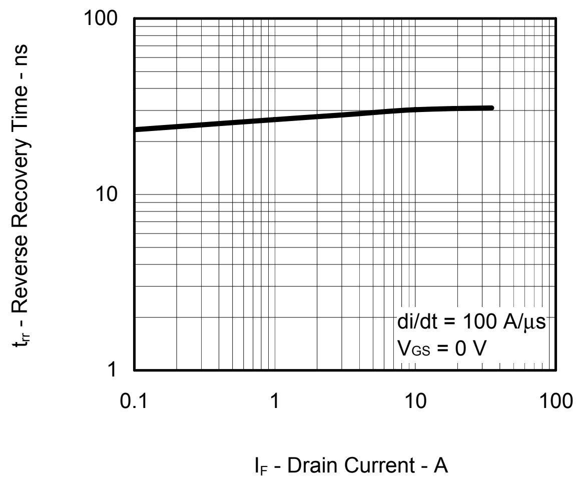
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

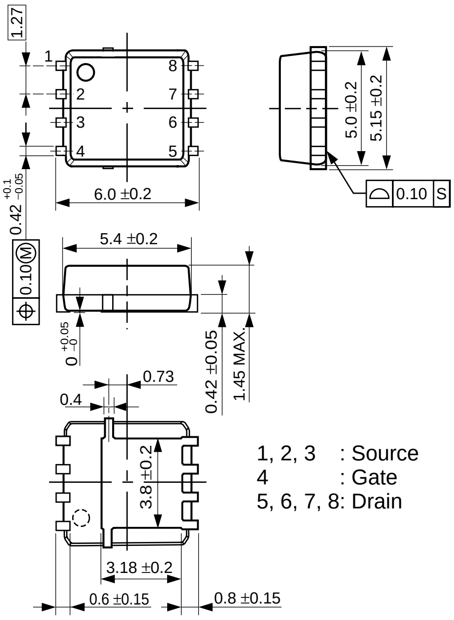


REVERSE RECOVERY TIME vs. DRAIN CURRENT

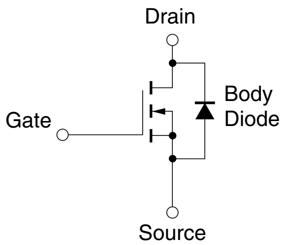


Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	NP35N04YUG

Rev.	Date	Description	
		Page	Summary
1.00	Jul 01, 2010	–	First Eddition Issued

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Refer to "http://www.renesas.com/" for the latest and detailed information.

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