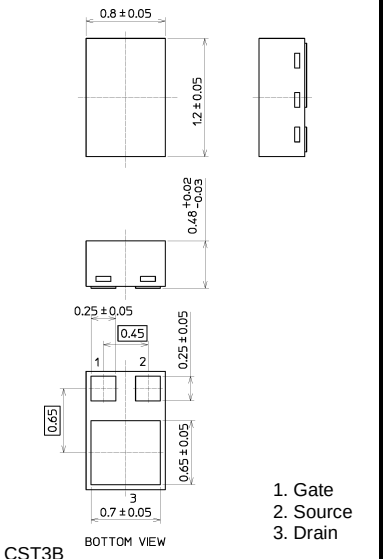
TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOS Ⅵ)

SSM3J46CTB

○ Power Management Switch Applications

- 1.5 V drive
- Low ON-resistance: $R_{DS(ON)}$ = 250 mΩ (max) (@V_{GS} = -1.5 V)
  $R_{DS(ON)}$ = 178 mΩ (max) (@V_{GS} = -1.8 V)
  $R_{DS(ON)}$ = 133 mΩ (max) (@V_{GS} = -2.5 V)
  $R_{DS(ON)}$ = 103 mΩ (max) (@V_{GS} = -4.5 V)

Unit: mm



CST3B

JEDEC	―
JEITA	―
TOSHIBA	2-1T1A

Weight: 1.5 mg (typ.)

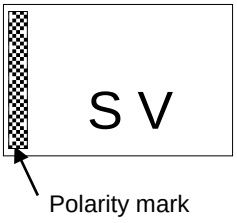
Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	-20	V
Gate-Source voltage		V_{GSS}	± 8	V
Drain current	DC	I_D	-2.0	A
	Pulse	I_{DP}	-4.0	
Power dissipation		P_D (Note 1)	1000	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

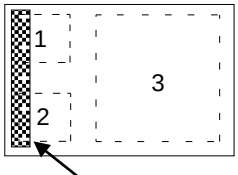
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on a FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Marking (top view)



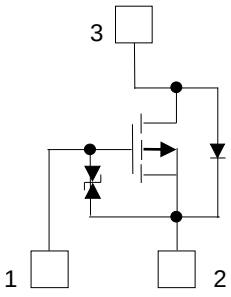
Pin Condition (top view)



1. Gate
2. Source
3. Drain

*Electrodes: on the bottom

Equivalent Circuit



Start of commercial production
2010-02

Electrical Characteristics (Ta = 25°C)

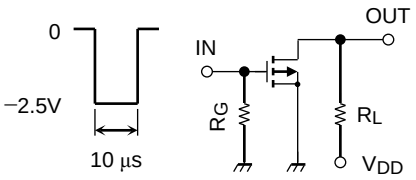
Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −1 mA, V_{GS} = 0 V	−20	—	—	V
		$V_{(BR)\ DSX}$	I_D = −1 mA, V_{GS} = 5 V (Note 3)	−15	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = −20 V, V_{GS} = 0 V	—	—	−1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = −3 V, I_D = −1 mA	−0.3	—	−1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −3 V, I_D = −1.0 A (Note 2)	—	5.2	—	S
Drain–source ON-resistance		$R_{DS\ (ON)}$	I_D = -1.5 A, V_{GS} = −4.5 V (Note 2)	—	88.5	103	mΩ
			I_D = -1.0 A, V_{GS} = −2.5 V (Note 2)	—	107.5	133	
			I_D = -0.5 A, V_{GS} = −1.8 V (Note 2)	—	130	178	
			I_D = -0.25 A, V_{GS} = −1.5 V (Note 2)	—	151	250	
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V f = 1 MHz	—	290	—	pF
Output capacitance		C_{oss}		—	44	—	
Reverse transfer capacitance		C_{rss}		—	32	—	
Switching time	Turn-on time	t_{on}	V_{DD} = −10 V, I_D = −0.5 A V_{GS} = 0 to −2.5 V, R_G = 4.7 Ω	—	13.4	—	ns
	Turn-off time	t_{off}		—	46.2	—	
Total Gate Charge		Q_g	V_{DD} = −10 V, I_D = −2.0 A, V_{GS} = − 4.5 V	—	4.7	—	nC
Gate-Source Charge		Q_{gs1}		—	0.4	—	
Gate-Drain Charge		Q_{gd}		—	1.0	—	
Drain-Source forward voltage		V_{DSF}	I_D = 2.0 A, V_{GS} = 0 V (Note 2)	—	0.9	1.2	V

Note2: Pulse test

Note3: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit

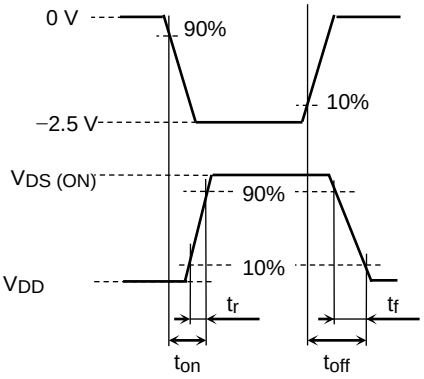
(a) Test Circuit



V_{DD} = -10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) VIN

(c) VOUT



Notice on Usage

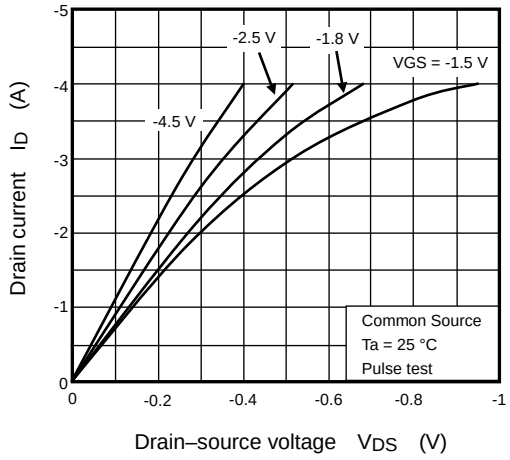
V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D = -1 mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

Take this into consideration when using the device.

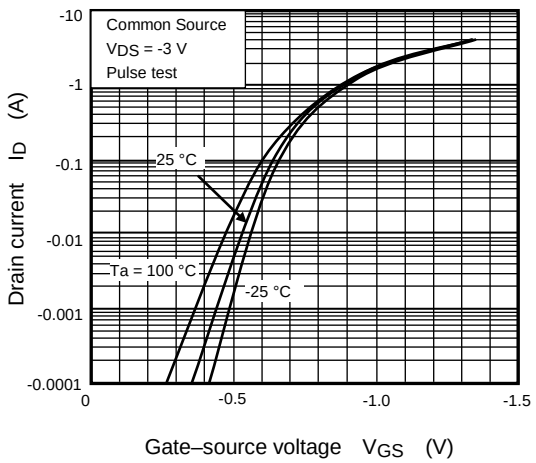
Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

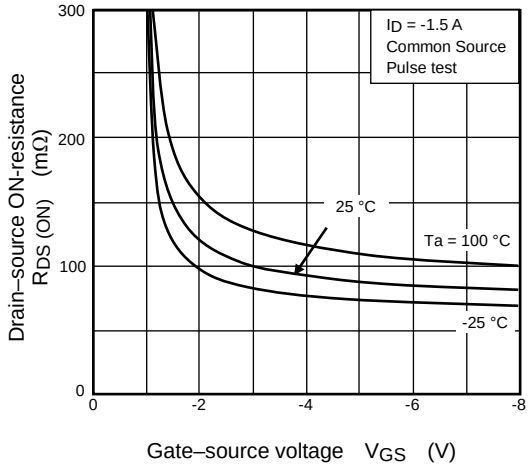
I_D – V_{DS}



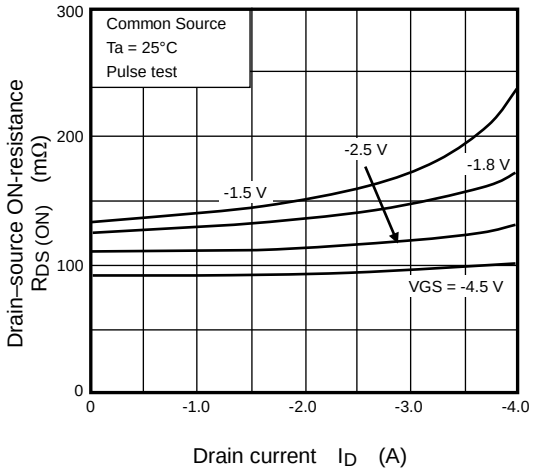
I_D – V_{GS}



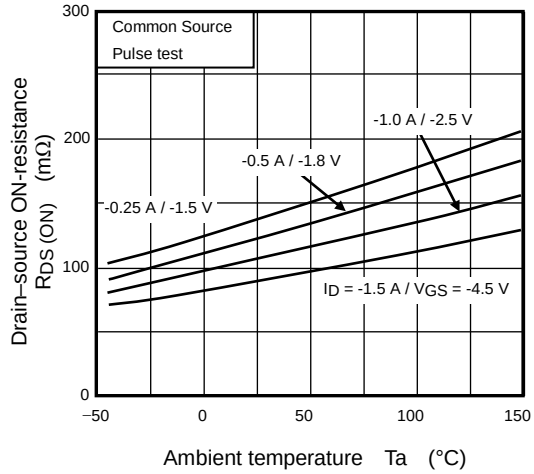
$R_{DS\ (ON)}$ – V_{GS}



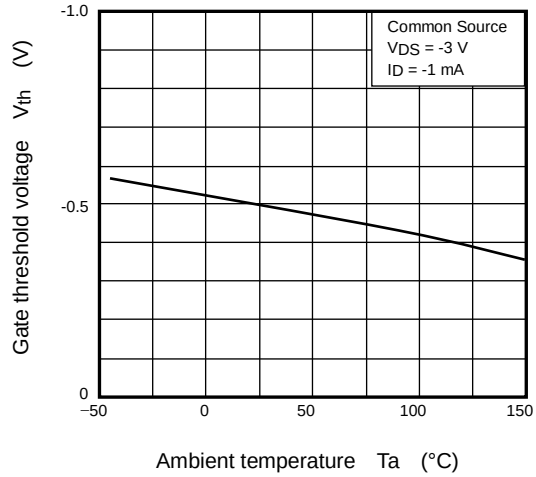
$R_{DS\ (ON)}$ – I_D

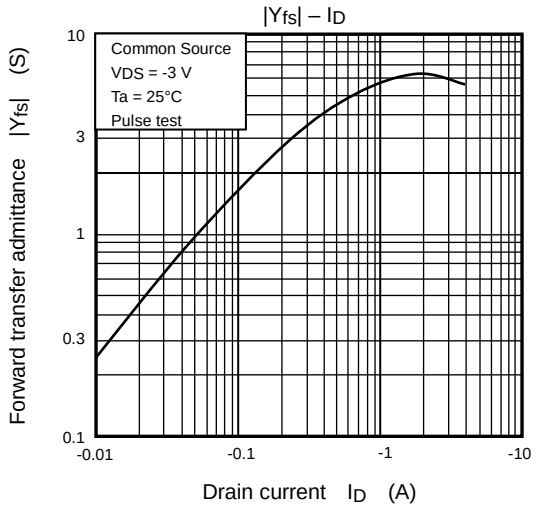


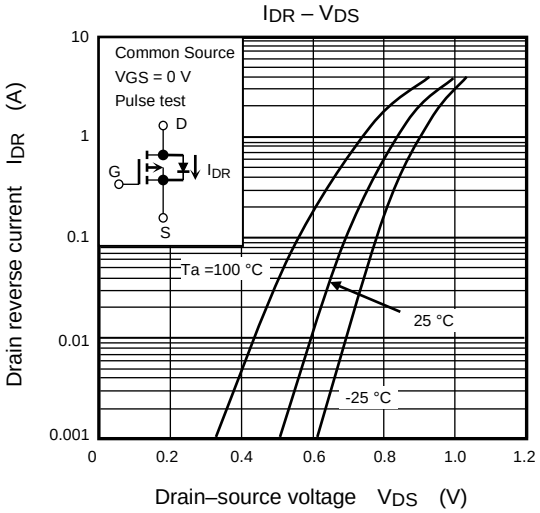
$R_{DS\ (ON)}$ – Ta

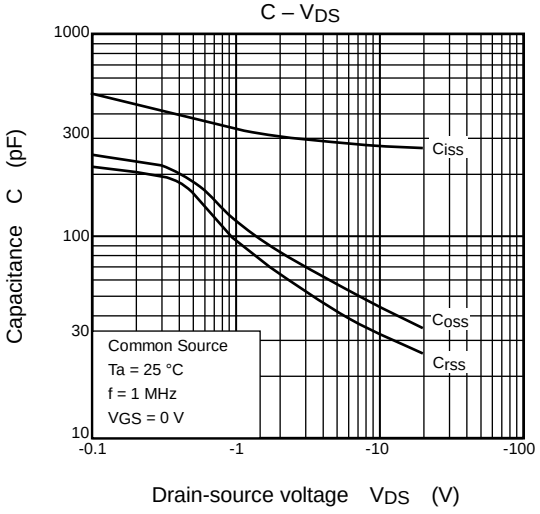


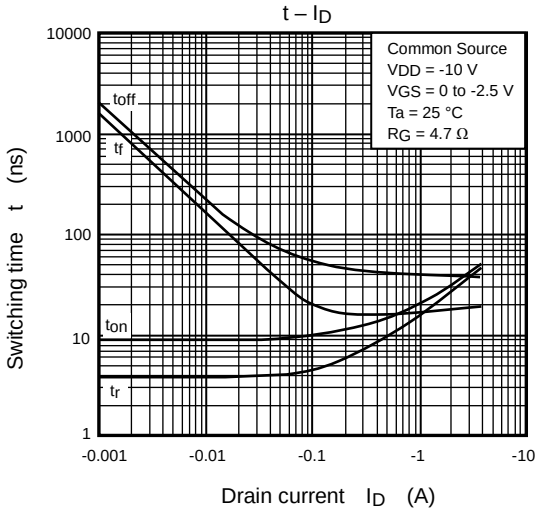
V_{th} – Ta

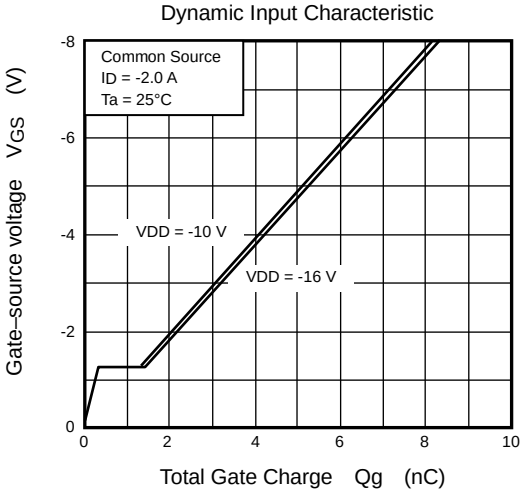



|Yfs| – ID
Common Source
VDS = -3 V
Ta = 25°C
Pulse test
Forward transfer admittance |Yfs| (S)
10
3
1
0.3
0.1
-0.01
-0.1
-1
-10
Drain current ID (A)

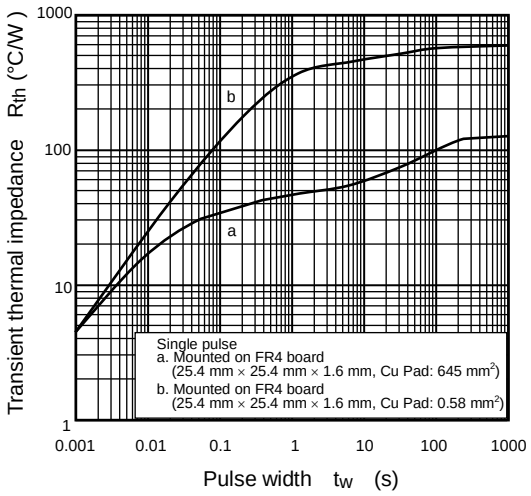

IDR – VDS
Common Source
VGS = 0 V
Pulse test
D
G
S
IDR
Drain reverse current IDR (A)
10
1
0.1
0.01
0.001
Ta =100 °C
25 °C
-25 °C
0
0.2
0.4
0.6
0.8
1.0
1.2
Drain–source voltage VDS (V)


C – VDS
Capacitance C (pF)
1000
300
100
30
10
Ciss
Coss
Crss
Common Source
Ta = 25 °C
f = 1 MHz
VGS = 0 V
-0.1
-1
-10
-100
Drain-source voltage VDS (V)

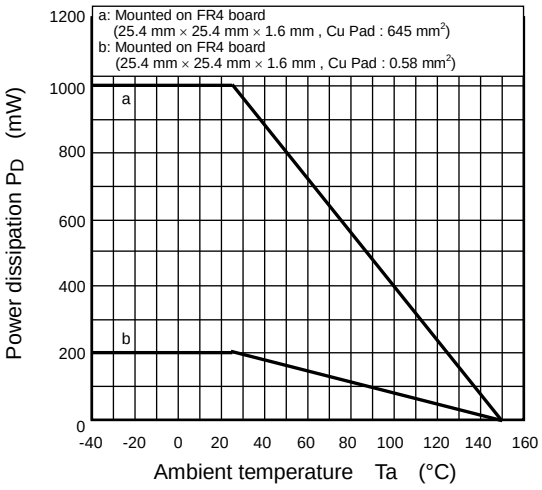

t – ID
Common Source
VDD = -10 V
VGS = 0 to -2.5 V
Ta = 25 °C
RG = 4.7 Ω
Switching time t (ns)
10000
1000
100
10
1
toff
tf
ton
tr
-0.001
-0.01
-0.1
-1
-10
Drain current ID (A)


Dynamic Input Characteristic
Common Source
ID = -2.0 A
Ta = 25°C
Gate–source voltage VGS (V)
-8
-6
-4
-2
0
VDD = -10 V
VDD = -16 V
0
2
4
6
8
10
Total Gate Charge Qg (nC)

$R_{th} – t_w$


Transient thermal impedance Rth (°C/W)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Pulse width tw (s)
b
a
Single pulse
a. Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm²)
b. Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.58 mm²)

$P_D – T_a$


Power dissipation PD (mW)
1200
1000
800
600
400
200
0
-40
-20
0
20
40
60
80
100
120
140
160
Ambient temperature Ta (°C)
a: Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm , Cu Pad : 645 mm²)
b: Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm , Cu Pad : 0.58 mm²)
a
b

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