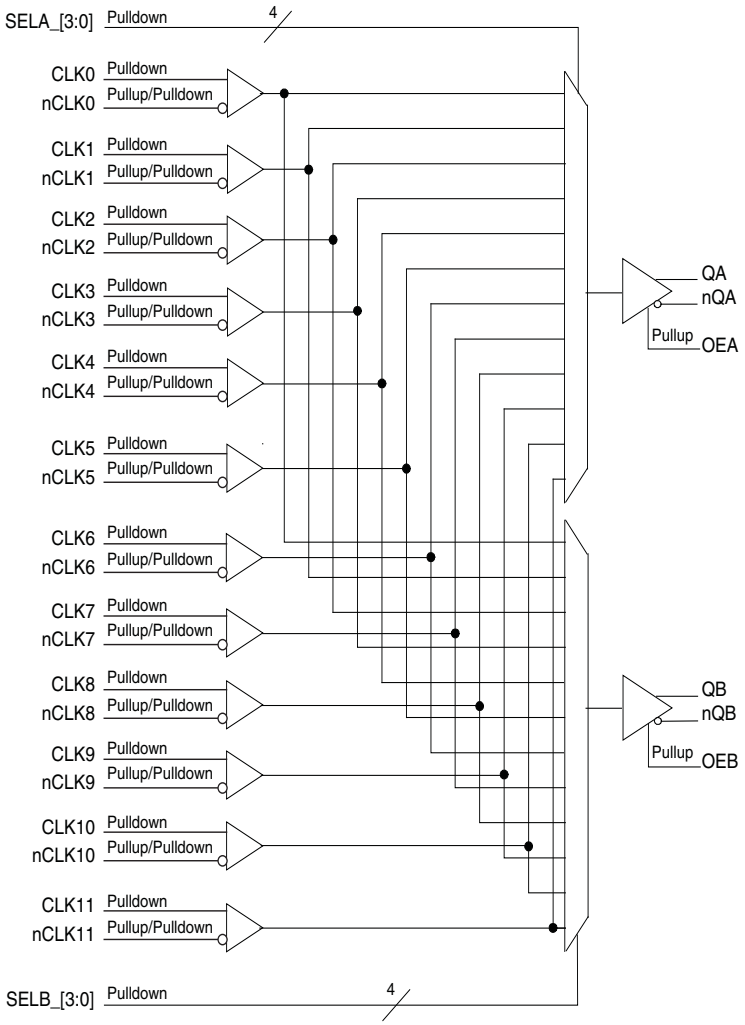
General Description

The ICS854S202I-01 is a 12:2 Differential-to-LVDS Clock Multiplexer which can operate up to 3GHz. The ICS854S202I-01 has twelve selectable differential clock inputs, any of which can be independently routed to either of the two LVDS outputs. The CLKx, nCLKx input pairs can accept LVPECL, LVDS or CML levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits.

Features

- Two differential 2.5V LVDS clock outputs
- Twelve selectable differential clock inputs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML
- Maximum output frequency: 3GHz
- Propagation delay: 1.1ns (maximum)
- Input skew: 100ps (maximum)
- Output skew: 50ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Additive phase jitter, RMS (12kHz – 20MHz): 0.16ps (typical)
- Full 2.5V operating supply mode
- -40°C to 85°C ambient operating temperature

Block Diagram



Pin Assignment

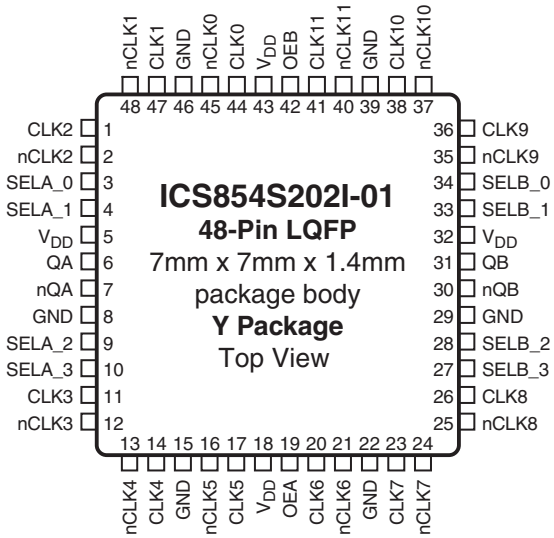


Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK2	Input	Pulldown	Non-inverting differential clock input.
2	nCLK2	Input	Pullup/Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
3, 4, 9, 10	SELA_0, SELA_1, SELA_2, SELA_3	Input	Pulldown	Clock select pins for Bank A output pair. See Control Input Function Table. LVCMOS/LVTTL interface levels. See Table 3B.
5, 18, 32, 43	V_{DD}	Power		Power supply pins.
6, 7	QA, nQA	Output		Clock outputs. LVDS interface levels.
8, 15, 22, 29, 39, 46	GND	Power		Power supply ground.
11	CLK3	Input	Pulldown	Non-inverting differential clock input.
12	nCLK3	Input	Pullup/Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
13	nCLK4	Input	Pullup/Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
14	CLK4	Input	Pulldown	Non-inverting differential clock input.
16	nCLK5	Input	Pullup/Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
17	CLK5	Input	Pulldown	Non-inverting differential clock input.
18, 43	V_{DD}	Power		Positive supply pins.
19	OEA	Input	Pullup	Output enable pin. Controls enabling and disabling of QA, nQA output pair. LVCMOS/LVTTL interface levels.
20	CLK6	Input	Pulldown	Non-inverting differential clock input.
21	nCLK6	Input	Pullup/Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
23	CLK7	Input	Pulldown	Non-inverting differential clock input.
24	nCLK7	Input	Pullup/Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
25	nCLK8	Input	Pullup/Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
26	CLK8	Input	Pulldown	Non-inverting differential clock input.
27, 28, 33, 34	SELB_3, SELB_2, SELB_1, SELB_0	Input	Pulldown	Clock select pins for Bank B output pair. See Control Input Function Table. LVCMOS/LVTTL interface levels. See Table 3C.
30, 31	nQB, QB	Output		Clock outputs. LVDS interface levels.
35	nCLK9	Input	Pullup/Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
36	CLK9	Input	Pulldown	Non-inverting differential clock input.
37	nCLK10	Input	Pullup/Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
38	CLK10	Input	Pulldown	Non-inverting differential clock input.
40	nCLK11	Input	Pullup/Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
41	CLK11	Input	Pulldown	Non-inverting differential clock input.
42	OEB	Input	Pullup	Output enable pin. Controls enabling and disabling of QB, nQB output pair. LVCMOS/LVTTL interface levels.
44	CLK0	Input	Pulldown	Non-inverting differential clock input.

Number	Name	Type		Description
45	nCLK0	Input	Pullup/Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
47	CLK1	Input	Pulldown	Non-inverting differential clock input.
48	nCLK1	Input	Pullup/Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3A. OEA, OEB Control Input Function Table

Input	Output
OEA, OEB	**QA, nQA, QB, nQB**
0	Disabled (Logic LOW)
1	Active (default)

Table 3B. SEL_A Control Input Function Table

Control Input				Input Selected to QA, nQA
SELA_3	SELA_2	SELA_1	SELA_0	
0	0	0	0	CLK0, nCLK0 (default)
0	0	0	1	CLK1, nCLK1
0	0	1	0	CLK2, nCLK2
0	0	1	1	CLK3, nCLK3
0	1	0	0	CLK4, nCLK4
0	1	0	1	CLK5, nCLK5
0	1	1	0	CLK6, nCLK6
0	1	1	1	CLK7, nCLK7
1	0	0	0	CLK8, nCLK8
1	0	0	1	CLK9, nCLK9
1	0	1	0	CLK10, nCLK10
1	0	1	1	CLK11, nCLK11
1	1	0	0	Output at logic LOW
1	1	0	1	Output at logic LOW
1	1	1	0	Output at logic LOW
1	1	1	1	Output at logic LOW

Table 3C. SEL_B Control Input Function Table

Control Input				Input Selected to QB, nQB
SELB_3	SELB_2	SELB_1	SELB_0	
0	0	0	0	CLK0, nCLK0 (default)
0	0	0	1	CLK1, nCLK1
0	0	1	0	CLK2, nCLK2
0	0	1	1	CLK3, nCLK3
0	1	0	0	CLK4, nCLK4
0	1	0	1	CLK5, nCLK5
0	1	1	0	CLK6, nCLK6
0	1	1	1	CLK7, nCLK7
1	0	0	0	CLK8, nCLK8
1	0	0	1	CLK9, nCLK9
1	0	1	0	CLK10, nCLK10
1	0	1	1	CLK11, nCLK11
1	1	0	0	Output at logic LOW
1	1	0	1	Output at logic LOW
1	1	1	0	Output at logic LOW
1	1	1	1	Output at logic LOW

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	70.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

Table 4A. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			110	128	ma

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	SELA_[3:0], SELB_[3:0]	V_{DD} = 2.625V			150	µA
		OEA, OEB	V_{DD} = 2.625V			10	µA
I_{IL}	Input Low Current	SELA_[3:0, SELB_[3:0]	V_{DD} = 2.625V, V_{IN} = 0V	-10			µA
		OEA, OEB	V_{DD} = 2.625V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK[0:11], nCLK[0:11]	V_{DD} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	CLK[0:11]	V_{DD} = 2.625V, V_{IN} = 0V	-10			µA
		nCLK[0:11]	V_{DD} = 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.5	V
V_{CMR}	Common Mode Input Voltage: NOTE 1, 2			GND + 0.5		V_{DD} – 0.7	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

Table 4D. LVDS DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.2		1.4	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

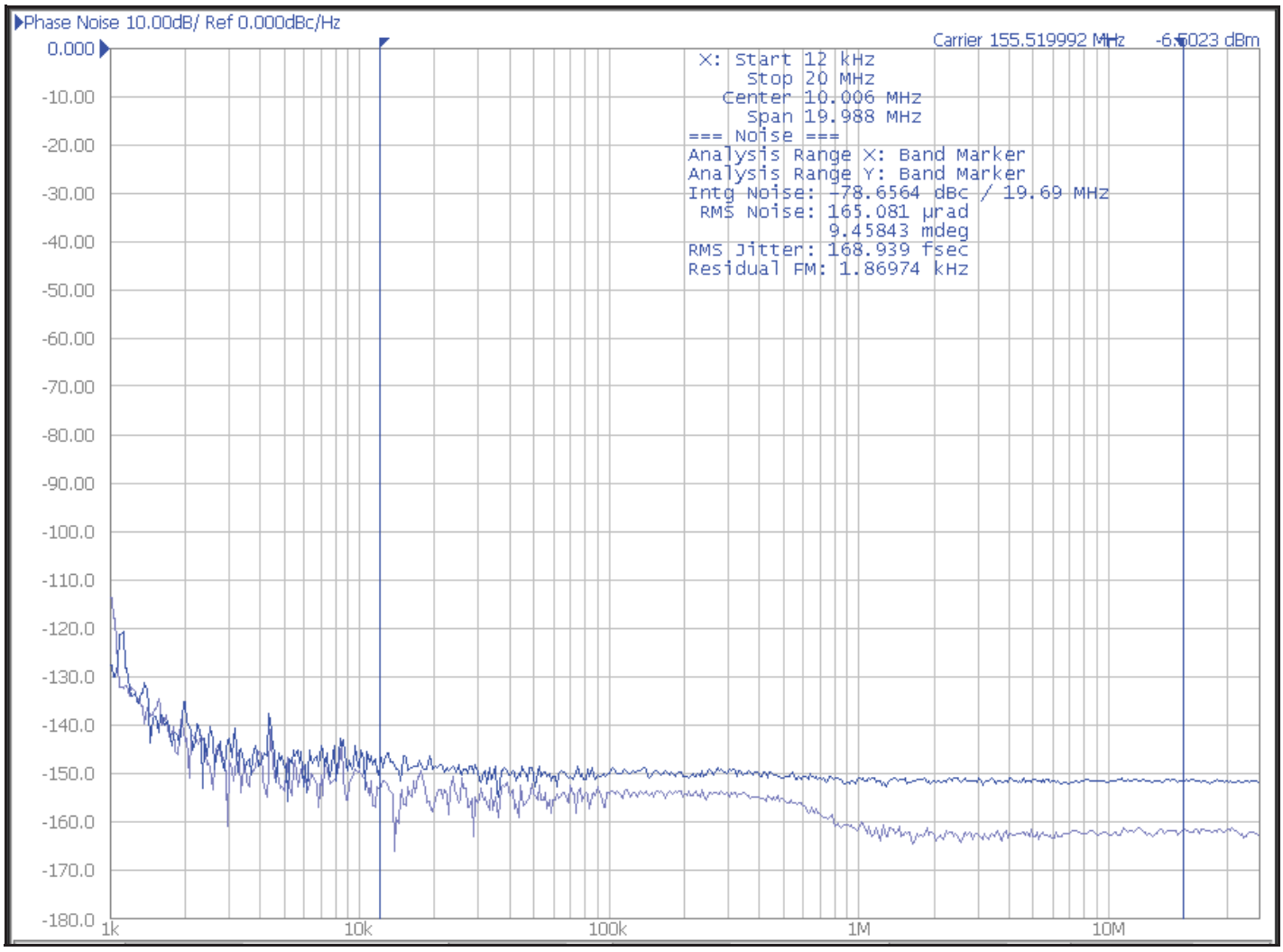
Table 5. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				3	GHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	f_{OUT} < 2GHz	450	660	1100	ps
		f_{OUT} > 2GHz	550	700	900	ps
tp_{HL}	Propagation Delay, High to Low; NOTE 1	f_{OUT} < 2GHz	450	660	1100	ps
		f_{OUT} > 2GHz	550	700	900	ps
*t*sk(o)	Output Skew; NOTE 2, 3			25	50	ps
*t*sk(i)	Input Skew; NOTE 3			25	100	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				250	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 5	155.52MHz, Integration Range: 12kHz - 20MHz		0.16	0.215	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50	110	250	ps
odc	Output Duty Cycle; NOTE 6		40	50	60	%
$MUX_{ISOLATION}$	MUX Isolation	f_{OUT} < 1.2GHz		75		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range. NOTE that phase noise may increase slightly with higher operating temperature. However, they will remain in spec as long as the maximum transistor junction temperature is not violated. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input cross point to the differential output cross point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential output cross point.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of input on each device, measured at the differential output cross point.
NOTE 5: Driving only one input clock.
NOTE 6: The output duty cycle will depend on the input duty cycle.

Additive Phase Jitter

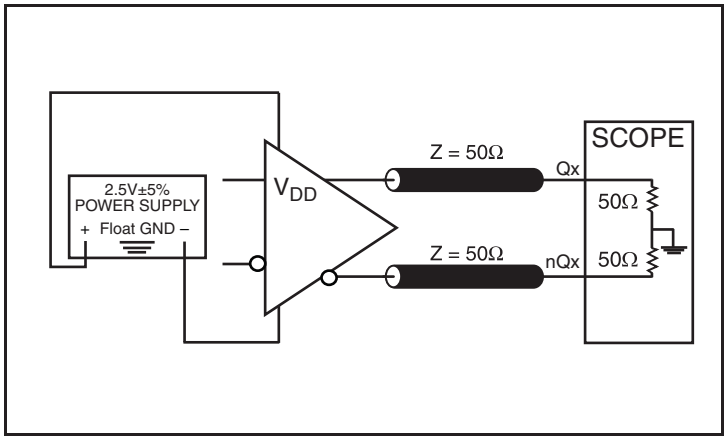
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise*. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



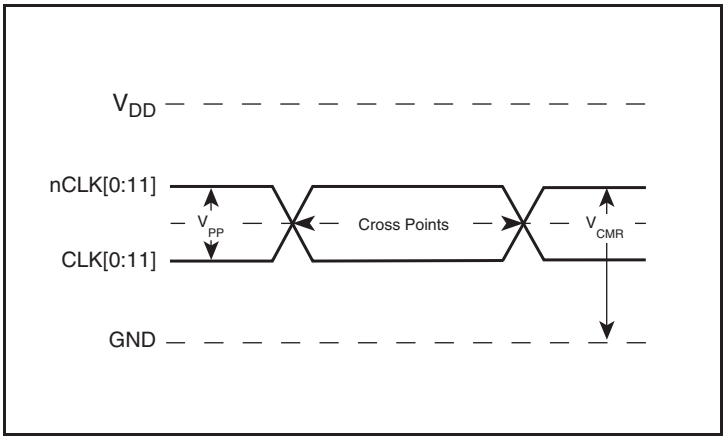
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Used the Rhode & Schwartz SMA100 as the input source.

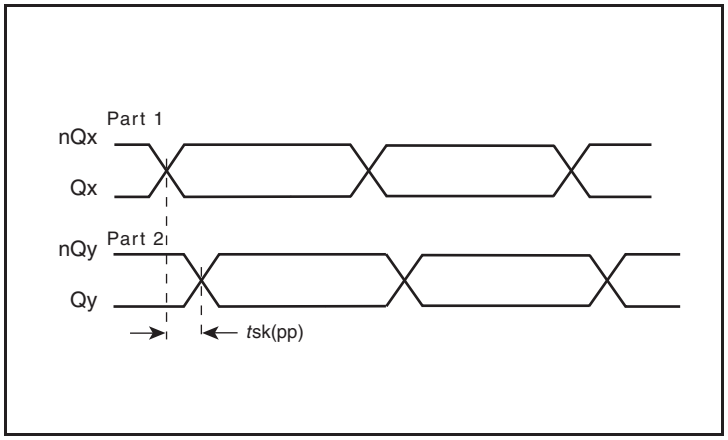
Parameter Measurement Information



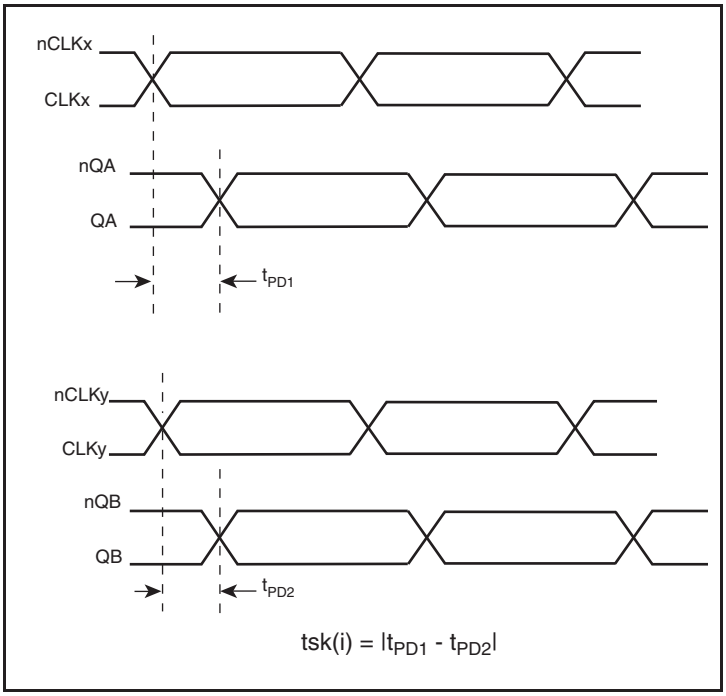
2.5V Output Load Test Circuit



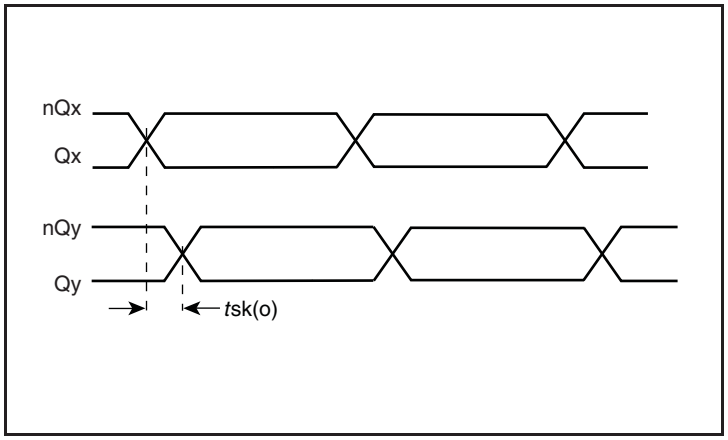
Differential Input Level



Part-to-Part Skew

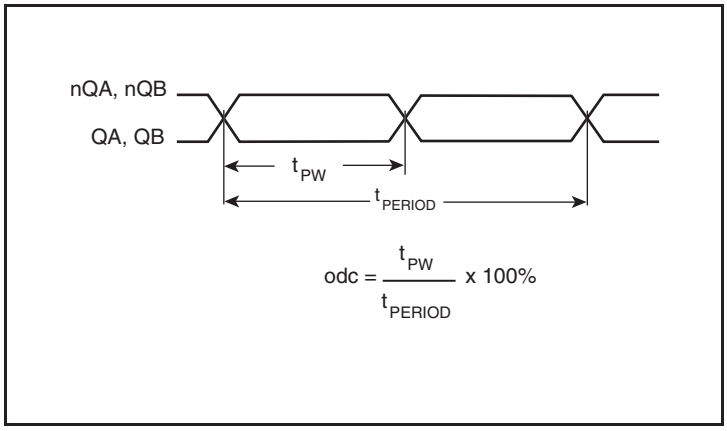


Input Skew

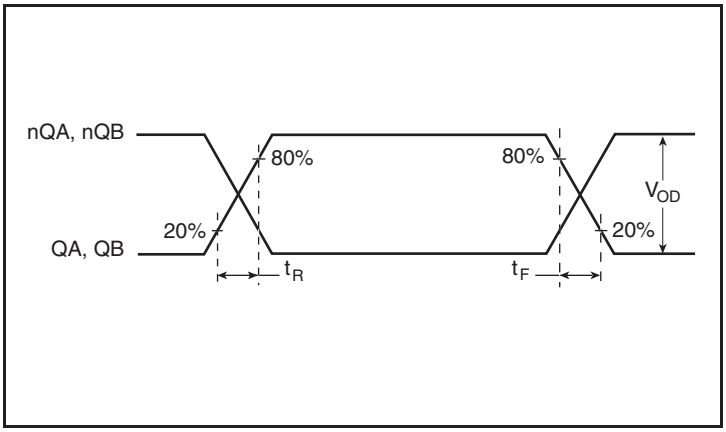


Output Skew

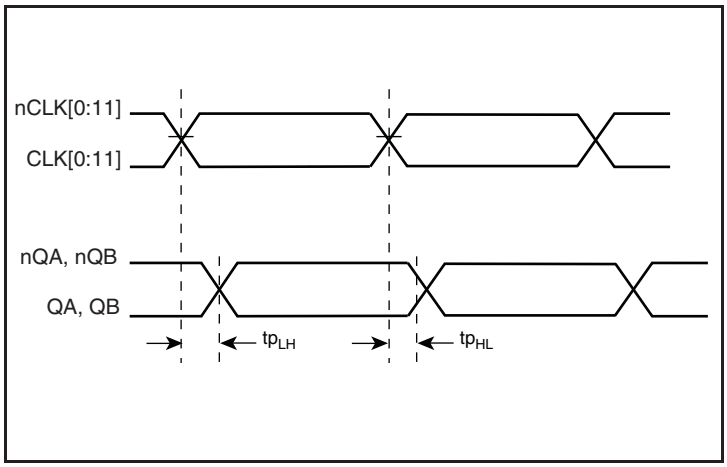
Parameter Measurement Information, continued



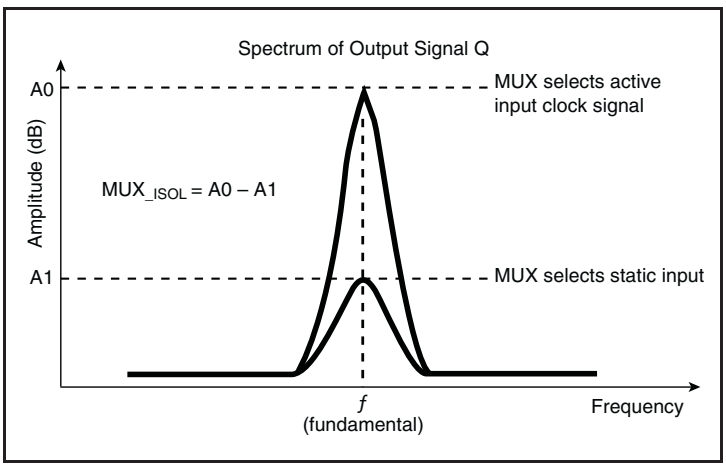
Output Duty Cycle/Pulse Width



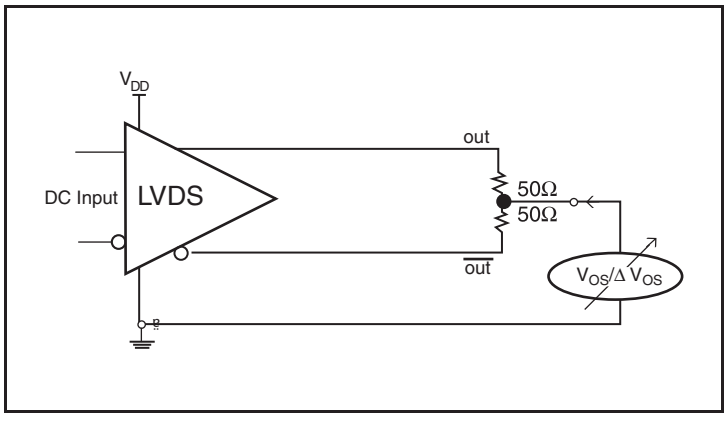
Output Rise/Fall Time



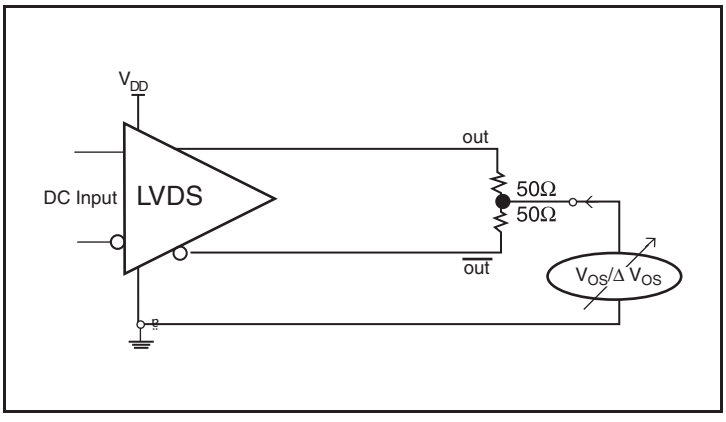
Propagation Delay



MUX Isolation



Differential Output Voltage Setup



Offset Voltage Setup

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications requiring only one differential input, the unused CLK and nCLK input can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK pin to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 2.5V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

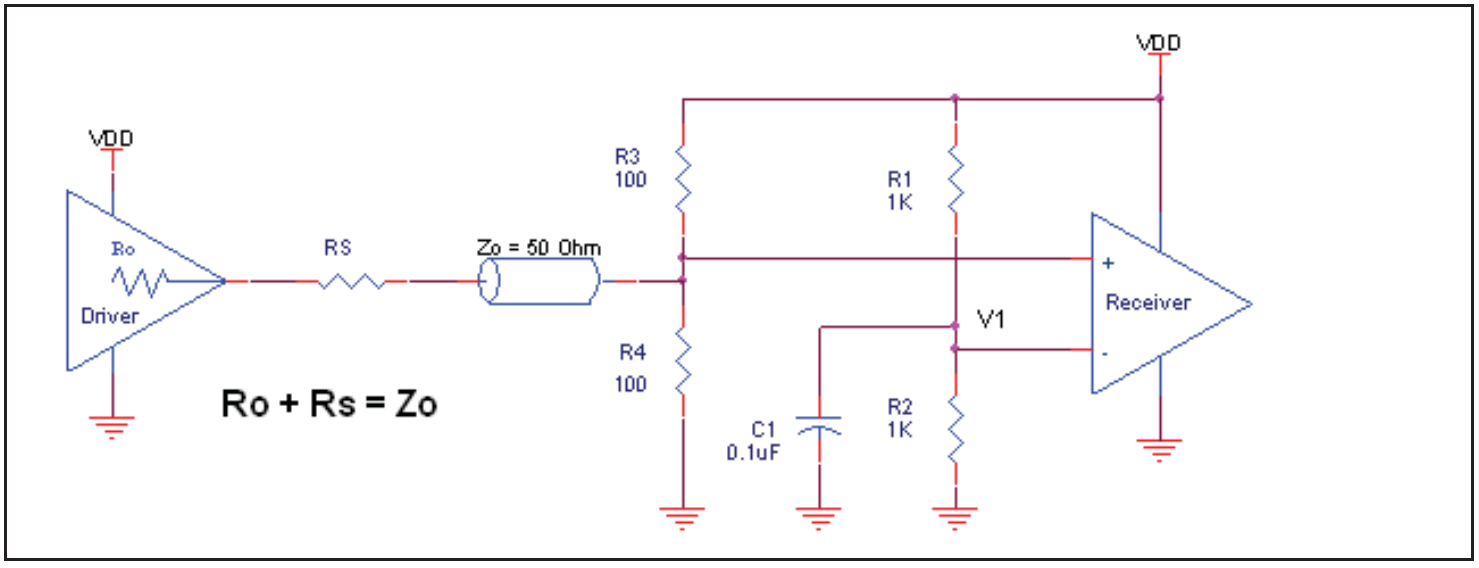


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, CML and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

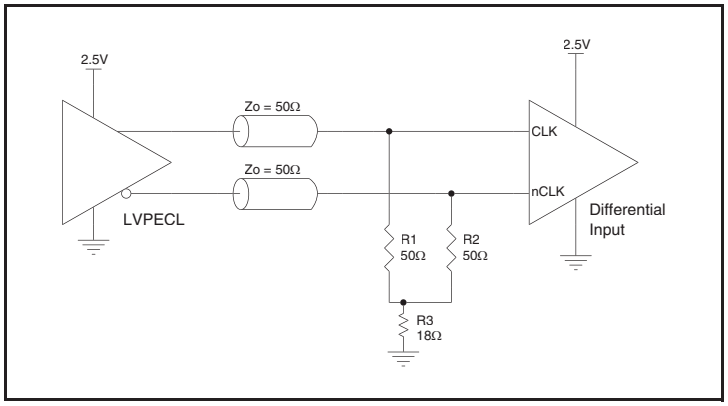


Figure 2A. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

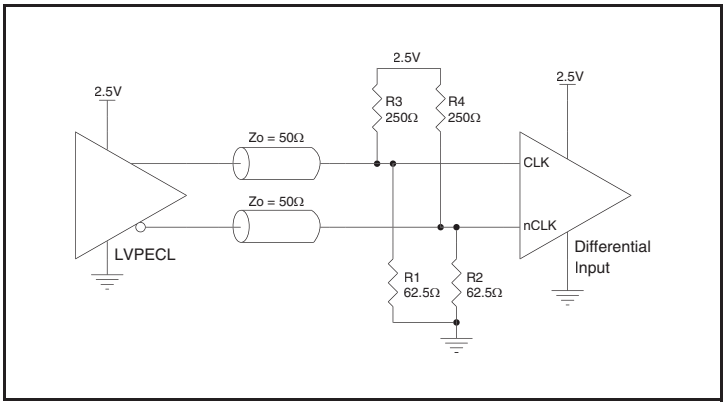


Figure 2B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

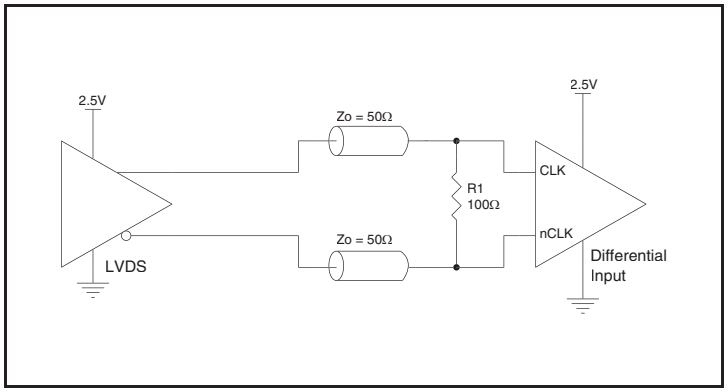


Figure 2C. CLK/nCLK Input Driven by a 2.5V LVDS Driver

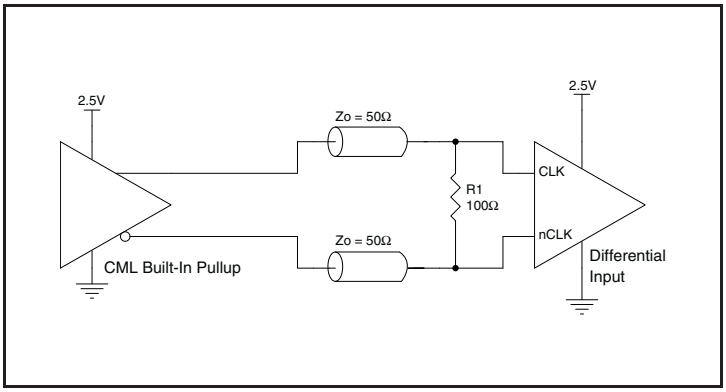


Figure 2D. CLK/nCLK Input Driven by a Built-In Pullup CML Driver

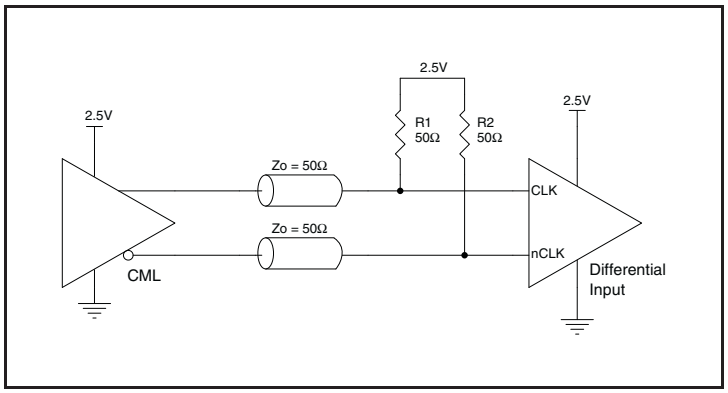


Figure 2E. CLK/nCLK Input Driven by an IDT Open Collector CML Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

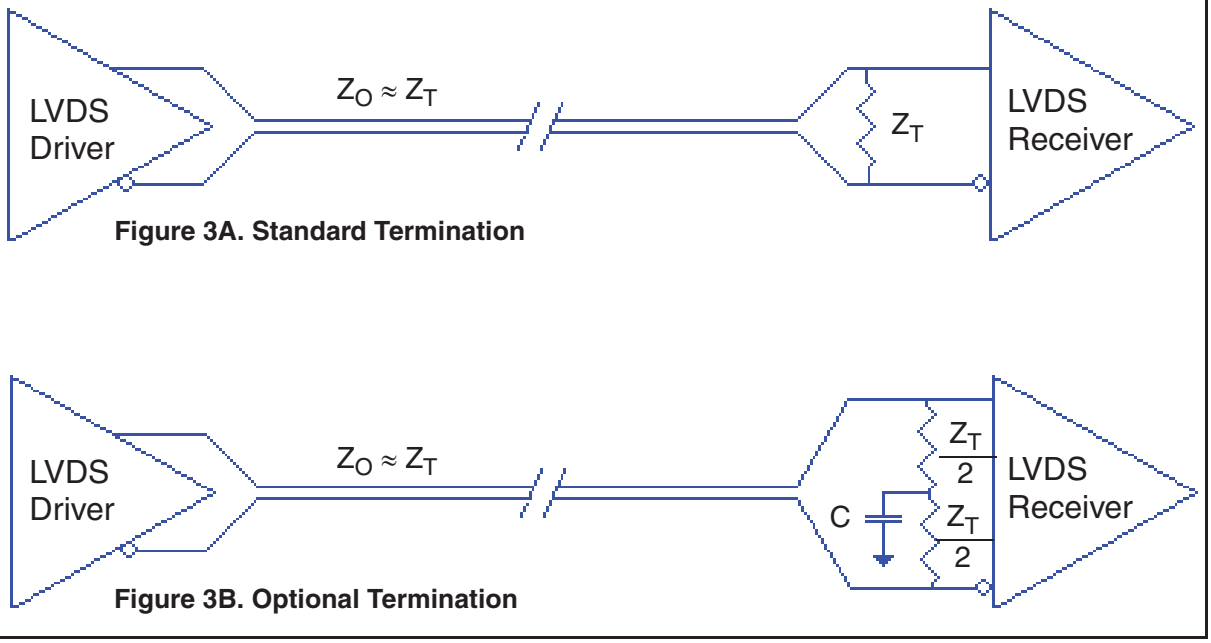


Figure 3A. Standard Termination

Figure 3B. Optional Termination

LVDS Termination

LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the ICS854S202I-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS854S202I-01 is the sum of the core power plus the output power dissipated due to the load.
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

- $Power_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 2.6255V * 128mA = **336mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 70.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.336W * 70.2°C/W = 108.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 48 Lead LQFP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70.2°C/W	60.4°C/W	56.9°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 48 Lead LQFP,

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70.2°C/W	60.4°C/W	56.9°C/W

Transistor Count

The transistor count for ICS854S202I-01 is: 8,537

Package Outline and Package Dimensions

Package Outline - Y Suffix for 48 Lead LQFP

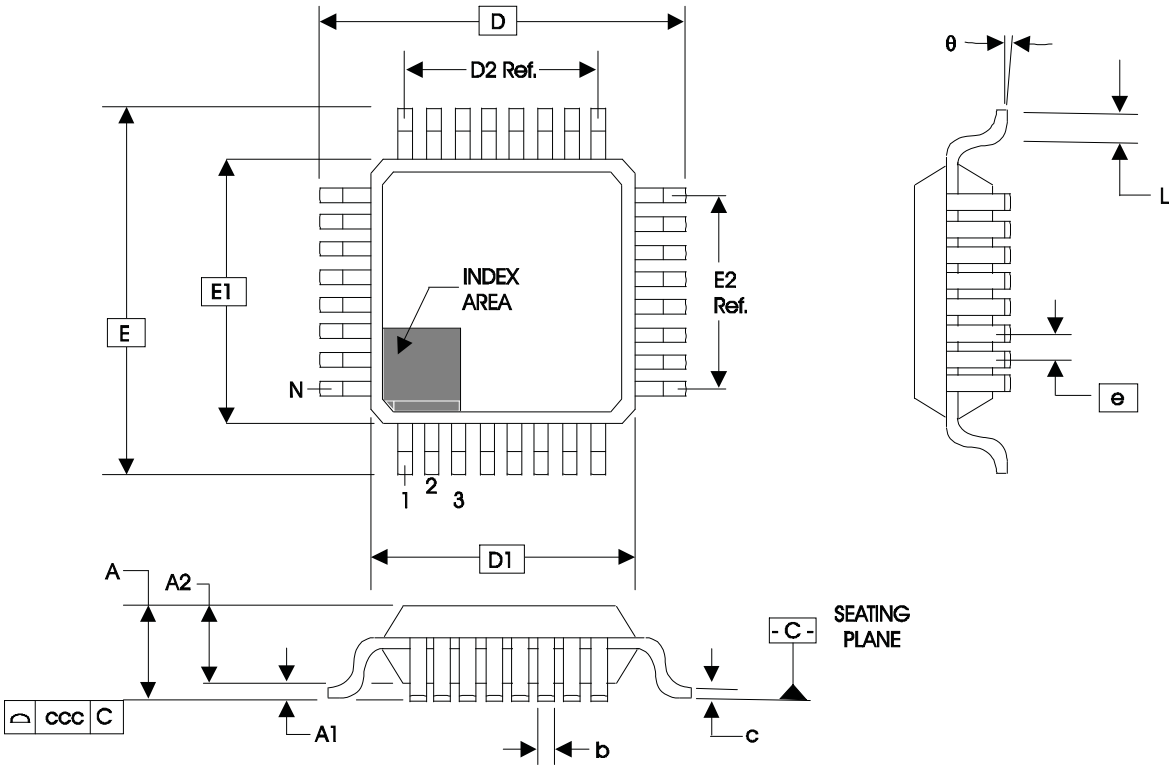


Table 8. Package Dimensions for 48 Lead LQFP

JEDEC Variation: BBC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		48	
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.50 Ref.	
e		0.5 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854S202AYI-01LF	ICSS202AI01L	“Lead-Free” 48 Lead LQFP	Tray	-40°C to 85°C
854S202AYI-01LFT	ICSS202AI01L	“Lead-Free” 48 Lead LQFP	Tape & Reel	-40°C to 85°C

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