PIC18F6525/6621/8525/8621 Rev. A1 Silicon/Data Sheet Errata

The PIC18F6525/6621/8525/8621 parts you have received conform functionally to the Device Data Sheet (DS39612**B**), except for the anomalies described below.

All the issues listed here will be addressed in future revisions of the PIC18F6525/6621/8525/8621 silicon.

The following silicon errata apply only to PIC18F6525/6621/8525/8621 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F6525	00 1010 111	00001
PIC18F6621	00 1010 101	00001
PIC18F8525	00 1010 110	00001
PIC18F8621	00 1010 100	00001

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2:DEVID1".

1. Module: EUSART

If the transmitter is left enabled while the module is performing an auto-baud operation, an arbitrary data byte may get transmitted.

Work around

Clear TXEN (TXSTAx<5>) before any auto-baud operation and set it after auto-baud is complete.

Enable TXEN only when a data byte is to be transmitted. Care must be taken to ensure that the TXx pin is pulled high, either through an external resistor, or by making the TXx pin an output and writing '1' to it to not disturb the transmit line.

2. Module: EUSART

This module may perform incorrect auto-baud calculation if the ABDEN (BAUDCONx<0>) bit was set while the receive pin was at a low level.

Work around

Wait for the RXx pin to go high and then set the ABDEN bit.

3. Module: EUSART

In Asynchronous Receiver mode, the EUSART does not load the SPBRGHx value after completion of auto-baud.

Work around

Do not enable the BRG16 (BAUDCONx<3>) bit.

If the BRG16 is in use, ensure that the auto-baud SPBRGx value does not exceed the 8-bit value.

4. Module: EUSART

The CREN (RCSTAx<4>) bit is cleared after every auto-baud operation.

Work around

Upon completion of auto-baud, manually set the CREN bit.

5. Module: A/D

An auto-acquisition A/D conversion requires a system clock source and can not be used in Sleep mode. If Sleep mode is entered during an auto-acquisition period, the A/D conversion will stop and the device will not wake-up. In addition, upon wake-up from other source, the result will not be valid.

Work around

Two work arounds exist:

1. Verify that the A/D conversion has completed before entering Sleep mode by confirming either the GO/$\overline{\text{DONE}}$ bit (ADCON0<1>) is '0' or the ADIF bit (PIR1<6>) is '1'.
2. Disable auto-acquisition by clearing the ACQT2:ACQT0 bits (ADCON2<5:3>) and use a software delay to acquire the sample.

6. Module: Core (Instruction Set)

The Decimal Adjust W register instruction, DAW, may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the DAW instruction. If the Carry bit is set, increment the next higher byte to be added using an instruction such as INCFSZ (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the DAW instruction has been executed, process the Carry bit normally (see Example 1).

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```
MOVLW   0x80        ; .80 (BCD)
ADDLW   0x80        ; .80 (BCD)

BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB
DAW
BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB
```

This is repeated for each DAW instruction.

7. Module: External Memory Bus

When performing writes on the external memory interface, a short glitch is present on the $\overline{LB}$ and $\overline{UB}$ lines. The length of the glitch is proportional to FOSC and also may vary with process, voltage and temperature. The glitch occurs well before the $\overline{WRH}$ line is asserted and no adverse affect on the operation of the external memory interface has been observed.

Work around

None

8. Module: EUSART

Bit SENDB in the TXSTAx register is not automatically cleared by hardware upon completion of transmission of a Sync Break.

Work around

Check the TRMT bit in TXSTAx. If TRMT bit is set, Break transmission is said to be complete.

9. Module: EUSART

Writing to the USART/EUSART TXREGx, faster than the baud rate in Synchronous mode, will overwrite the previous value instead of double-buffering as in Asynchronous mode.

Work around

Load the first character into TXREGx and then wait for a TXx interrupt, or check the TXxIF bit before writing each additional character to TXREGx.

10. Module: EUSART

The EUSART cannot receive asynchronous data at the four fastest baud rates (BRGH = 1, BRG16 = 1 and SPBRGx < 4).

Work around

Use a slower baud rate or a faster system clock speed.

11. Module: EUSART

The EUSART for PIC18F8525/8621 devices may not recognize a received Stop bit if the combined error rate is too high.

Work around

1. Increase the baud rate of the device by decrementing the SPBRGHx:SPBRGx register pair value by one. Verify that the new baud rate does not exceed the maximum combined error rate of the application.
2. Configure the transmitter to send two Stop bits.

12. Module: Core

Certain combinations of code sequence, code placement, VDD, FOSC and temperature may cause a corrupted read of fetched instructions or data. A corrupted instruction fetch will cause the part to execute an incorrect instruction with unpredictable results.

Microchip cannot predict which combinations of these conditions will cause this failure.

If this failure mechanism exists in your system, it should become evident during statistically significant preproduction testing, using your particular code sequence and placement, across multiple date codes.

Preproduction testing should exercise all the functions of your application across system variables. Any changes to code should be tested in the same manner prior to being implemented.

Work around

- Migrate to an equivalent part in the PIC18F8622 product family
- If migrating to the PIC18F8622 product family is not feasible, try changing the placement of code within program memory. Examples of code placement changes include:
  - Insert a data word of value FFFFh immediately following any table read instruction
  - Insert a data word of value FFFFh as the first instruction in the destination of a CALL or GOTO
  - Insert a data word of FFFFh at the interrupt vector address(es) (0008h and/or 0018h)
  - Insert a data word of value FFFFh immediately following any RETURN, RETLW, or RETFIE instruction

In each of these instances, the literal data behaves as a NOP instruction when it is executed. Using the actual NOP instruction instead of a literal FFFFh may not have the same results.

After making any of the changes described above, it is necessary that you do statistically significant preproduction testing, using your new code sequence and placement, across multiple date codes.

Preproduction testing should exercise all the functions of your application across system variables.

- Contact your nearest Microchip sales office for additional help.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39612**B**), the following clarifications and corrections should be noted.

None.

REVISION HISTORY

Rev A Document (7/2003)
First revision of this document, silicon issues 1 through 4 (EUSART), 5 (ADC) and 6 (Core).

Rev B Document (2/2004)
Added silicon issues 7 (External Memory Bus) and 8-10 (EUSART) and Data Sheet Clarification issue 1 (External Memory Interface).

Rev C Document (1/2005)
Revised silicon issue 5 (A/D) and added silicon issue 11 (EUSART). Removed Data Sheet Clarification issue 1 (External Memory Interface).

Rev D Document (12/2006)
Added silicon issue 12 (Core).

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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