# AO6411

## 20V P-Channel AlphaMOS

## General Description

- Trench Power AlphaMOS (αMOS LV) technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

## Applications

- Load switch
- Battery protection

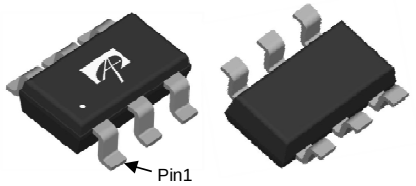
## Product Summary

| | |
|---|---|
| $V_{DS}$ | -20V |
| $I_D$ (at $V_{GS}$=-4.5V) | -7A |
| $R_{DS(ON)}$ (at $V_{GS}$=-4.5V) | < 28.5mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$=-2.5V) | < 36.5mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$=-1.8V) | < 47 mΩ |

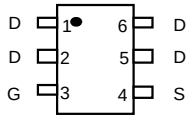
Green Product

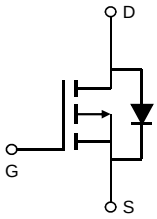
TSOP6

Top View Bottom View




Top View




| Orderable Part Number | Package Type | Form | Minimum Order Quantity |
|---|---|---|---|
| AO6411 | TSOP-6 | Tape & Reel | 3000 |

**Absolute Maximum Ratings $T_A$=25℃ unless otherwise noted**

| Parameter | | Symbol | Maximum | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±8 | V |
| Continuous Drain Current | $T_A$=25℃ | $I_D$ | -7 | A |
| | $T_A$=70℃ | | -5.5 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | -28 | |
| Power Dissipation [B] | $T_A$=25℃ | $P_D$ | 2.7 | W |
| | $T_A$=70℃ | | 1.7 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | ℃ |

**Thermal Characteristics**

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 35 | 45 | ℃/W |
| Maximum Junction-to-Ambient [A D] | Steady-State | | 60 | 75 | ℃/W |
| Maximum Junction-to-Lead | Steady-State | $R_{\theta JL}$ | 23 | 30 | ℃/W |

**Electrical Characteristics ($T_J$=25°C unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | ID=-250µA, $V_{GS}$=0V | -20 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=-20V, $V_{GS}$=0V | | | -1 | µA |
| | | $T_J$=55°C | | | -5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$=±8V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS,}$ $I_D$=-250µA | -0.3 | -0.65 | -0.9 | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=-4.5V, $I_D$=-7A | | 23.5 | 28.5 | mΩ |
| | | $T_J$=125°C | | 34 | 41 | |
| | | $V_{GS}$=-2.5V, $I_D$=-3.5A | | 29 | 36.5 | mΩ |
| | | $V_{GS}$=-1.8V, $I_D$=-2.2A | | 36 | 47 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=-5V, $I_D$=-7A | | 23 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=-1A, $V_{GS}$=0V | | -0.62 | -1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | -3.5 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=-10V, f=1MHz | | 1025 | | pF |
| $C_{oss}$ | Output Capacitance | | | 167 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 119 | | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | | 11 | | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$ | Total Gate Charge | $V_{GS}$=-4.5V, $V_{DS}$=-10V, $I_D$=-7A | | 13 | 18 | nC |
| $Q_{gs}$ | Gate Source Charge | | | 2 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 3.4 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=-4.5V, $V_{DS}$=-10V, $R_L$=1.43Ω, $R_{GEN}$=3Ω | | 10 | | ns |
| $t_r$ | Turn-On Rise Time | | | 15 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 85 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 40 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=-7A, di/dt=500A/µs | | 30 | | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=-7A, di/dt=500A/µs | | 80 | | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial$T_J$=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

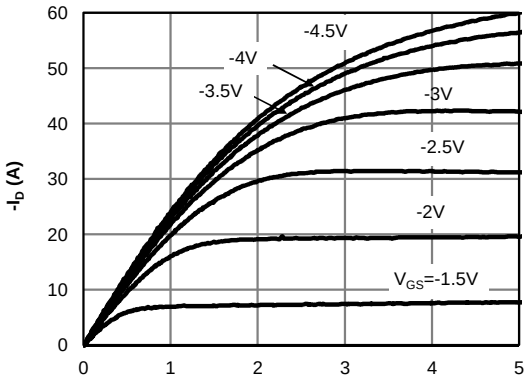



**Figure 1: On-Region Characteristics (Note E)**

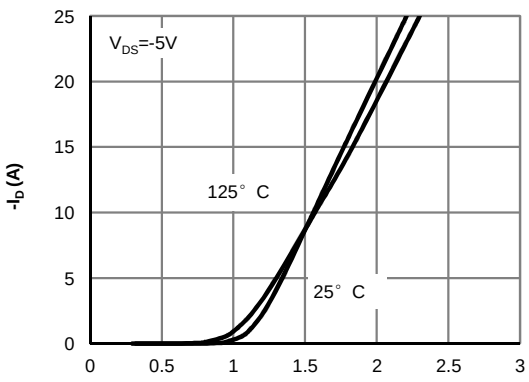



**Figure 2: Transfer Characteristics (Note E)**

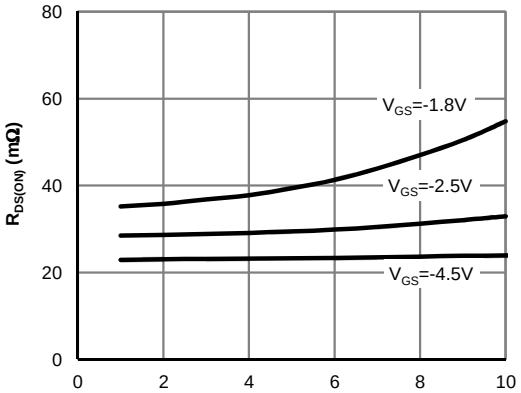



**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**

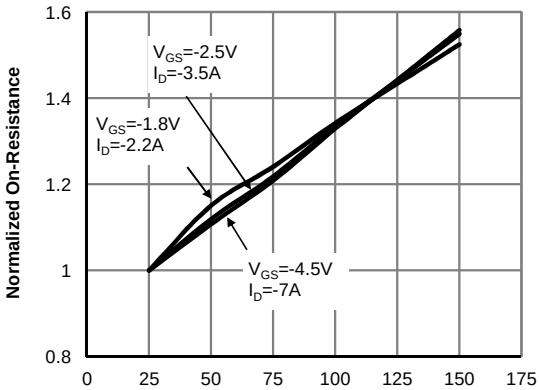



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

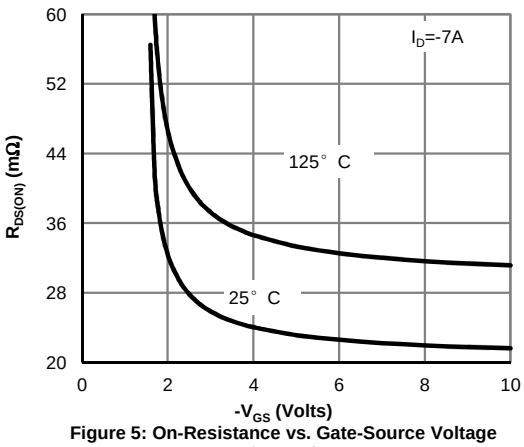



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

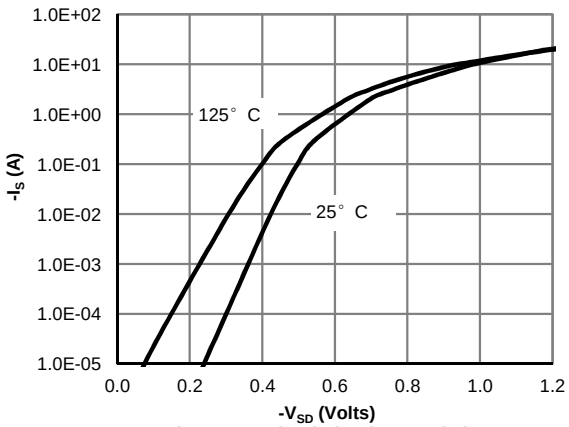



**Figure 6: Body-Diode Characteristics (Note E)**

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

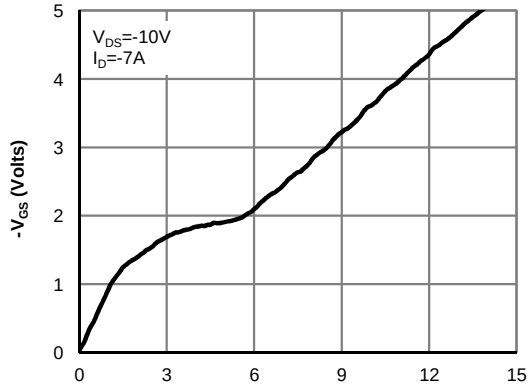



**Figure 7: Gate-Charge Characteristics**

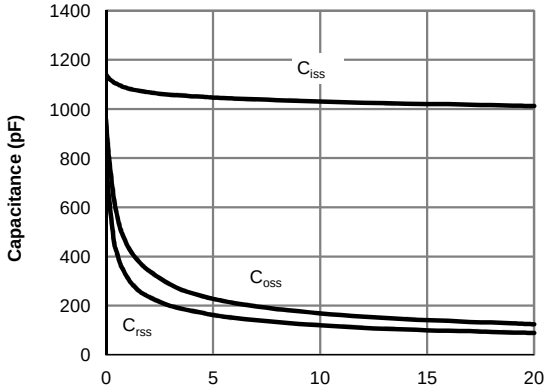
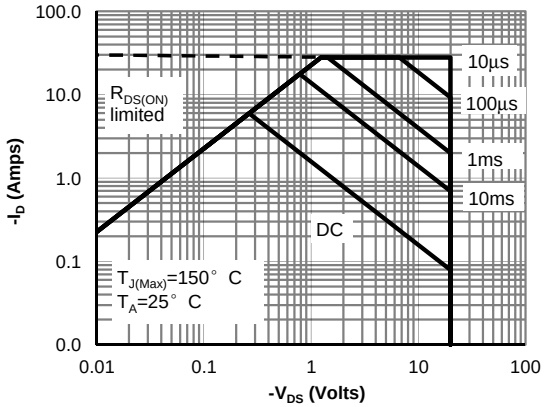



**Figure 8: Capacitance Characteristics**




$V_{GS}$<or equal to -1.8V

**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

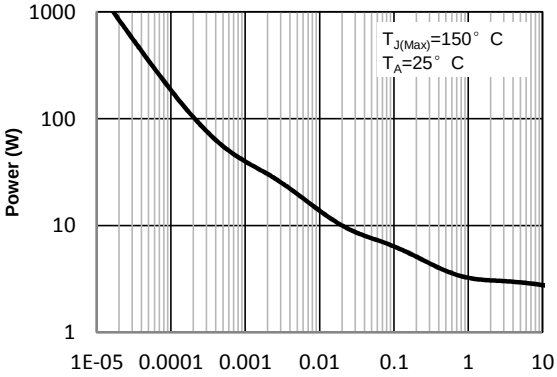



**Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)**

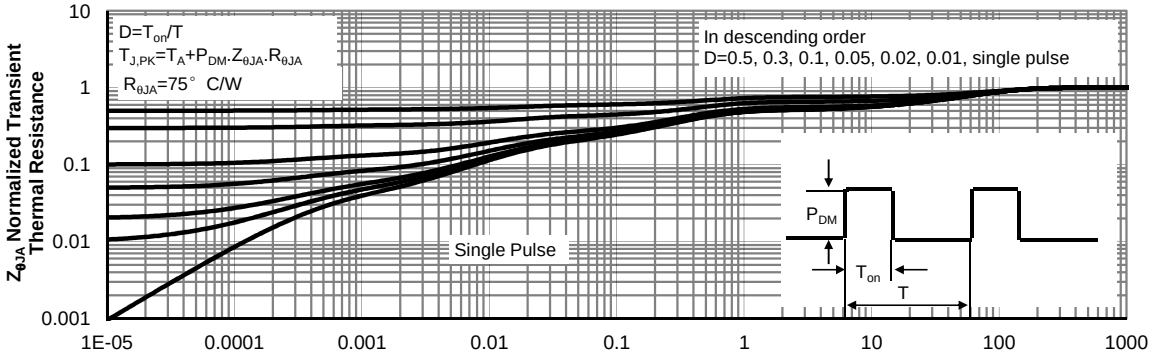
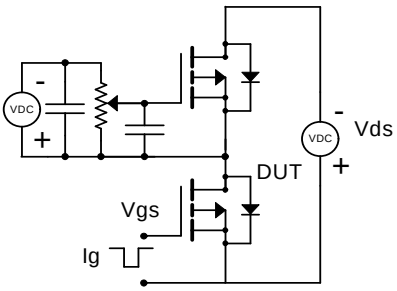
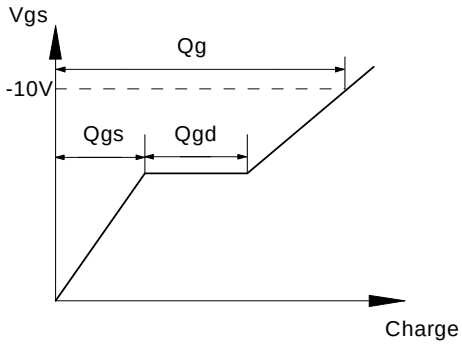


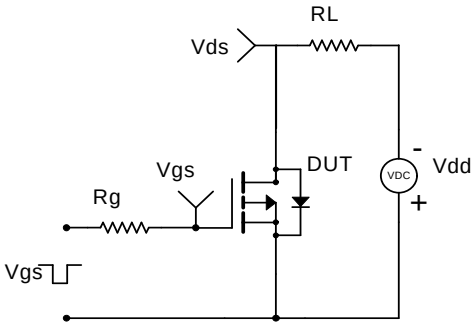

**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

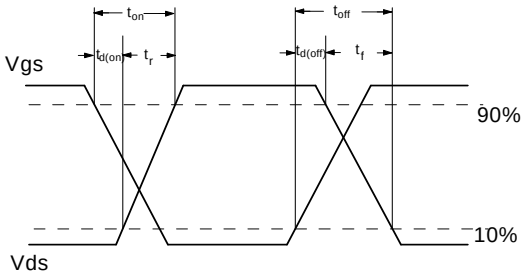
## Gate Charge Test Circuit & Waveform



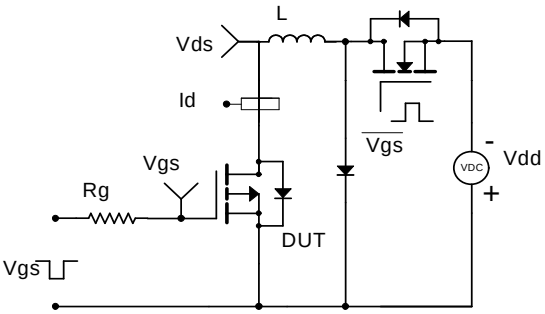



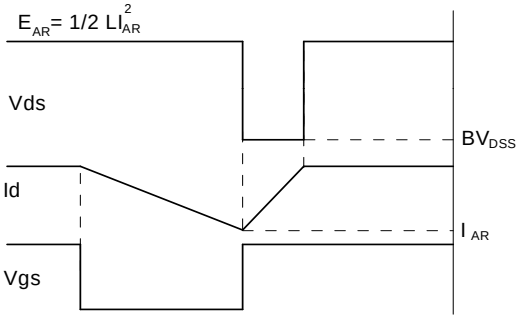

## Resistive Switching Test Circuit & Waveforms




## Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




## Diode Recovery Test Circuit & Waveforms