BLF4G22-130; BLF4G22LS-130

UHF power LDMOS transistor

Rev. 01 — 3 July 2007 Product data sheet

1. Product profile

1.1 General description

130 W LDMOS power transistor for base station applications at frequencies from 2000 MHz to 2200 MHz.

Table 1. Typical performance

T_{case} = 25 °C in a common source class-AB test circuit.

Mode of operation	f (MHz)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	IMD3 (dBc)	ACPR (dBc)
2-carrier W-CDMA[1]	f_1 = 2135; f_2 = 2145	28	33	13.5	26	–37	–41

[1] 10 MHz carrier spacing PAR 7 dB at 0.01 % probability on CCDF, 3GPP test model 1, 1 - 64 DPCH.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

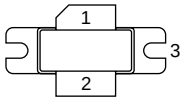
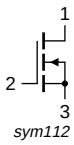
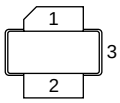
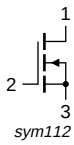
- Typical 2-carrier W-CDMA performance at a supply voltage of 28 V and an I_{Dq} of 1150 mA:
  - Average output power = 33 W
  - Power gain = 13.8 dB
  - Efficiency = 26 %
  - ACPR = –41 dBc
  - IMD3 = –37 dBc
- Easy power control
- Integrated ESD protection
- Excellent ruggedness (> 10 : 1 VSWR at 130 W (CW))
- High efficiency
- High peak power capability (> 190 W)
- Excellent thermal stability
- Designed for broadband operation (2000 MHz to 2200 MHz)
- Internally matched for ease of use

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 2000 MHz to 2200 MHz frequency range.

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Symbol
BLF4G22-130 (SOT502A)				
1	drain			
2	gate			
3	source	[1]		
BLF4G22LS-130 (SOT502B)				
1	drain			
2	gate			
3	source	[1]		

sym112

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF4G22-130	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF4G22LS-130	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+15	V
I_D	drain current		-	15	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Type	Typ	Max	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 33 W	BLF4G22-130	0.56	0.65	K/W
			BLF4G22LS-130	0.50	0.59	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.1 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 230 mA	2.5	3.1	3.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	5	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 6 V; V_{DS} = 10 V	35	44	-	A
I_{GSS}	gate leakage current	V_{GS} = +15 V; V_{DS} = 0 V	-	-	420	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 12.8 A	-	11	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 6 V; I_D = 7.7 A	-	0.07	-	Ω
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz	-	3.4	-	pF

7. Application information

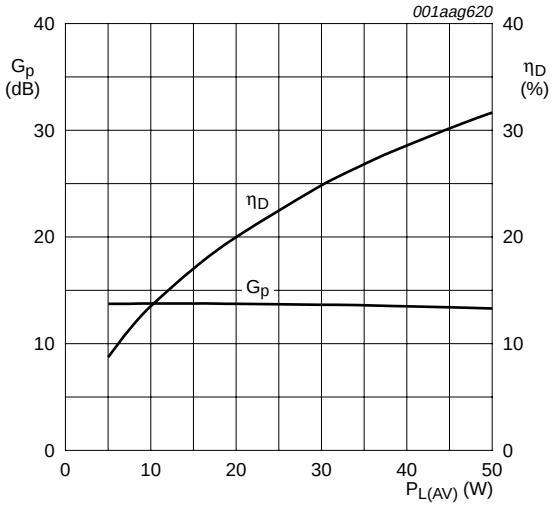
Table 7. Application information

Mode of operation: 2-carrier W-CDMA, PAR 7 dB at 0.01 % probability on CCDF; 3GPP test model 1, 1-64 DPCH; f_1 = 2112.5 MHz; f_2 = 2122.5 MHz; f_3 = 2157.5 MHz; f_4 = 2167.5 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 33 W	12.5	13.5	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 33 W	–9	–15	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 33 W	24	26	-	%
IMD3	third order intermodulation distortion	$P_{L(AV)}$ = 33 W	-	–37	–34	dBc
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 33 W	-	–41	–39	dBc

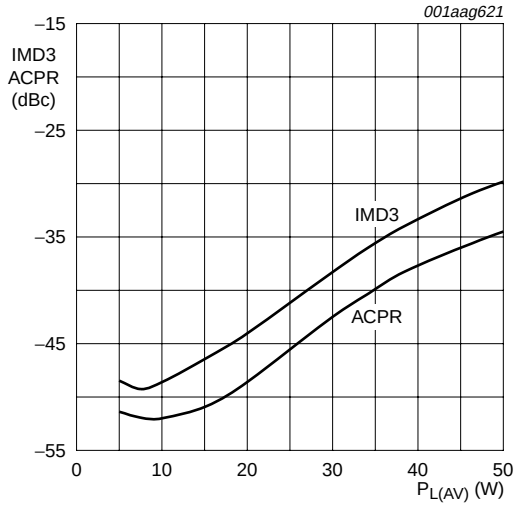
7.1 Ruggedness in class-AB operation

The BLF4G22-130 and the BLF4G22LS-130 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 1150 mA; P_L = 130 W (CW).



V_{DS} = 28 V; I_{Dq} = 900 mA; T_{case} = 25 °C;
f = 1990 MHz.

Fig 1. 2-Carrier W-CDMA power gain and drain efficiency as functions of average load power; typical values



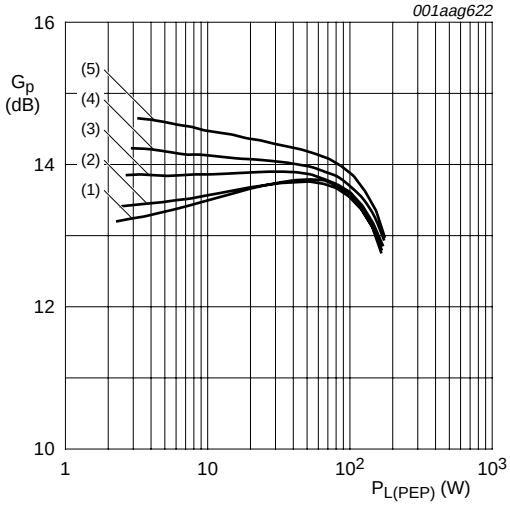
V_{DS} = 28 V; I_{Dq} = 900 mA; T_{case} = 25 °C;
f = 1990 MHz.

Fig 2. 2-Carrier W-CDMA IMD3 and ACPR as functions of average load power; typical values

Table 8. Typical impedance

V_{DS} = 28 V; I_{Dq} = 1150 mA; $P_{L(AV)}$ = 33 W; T_{case} = 25 °C.

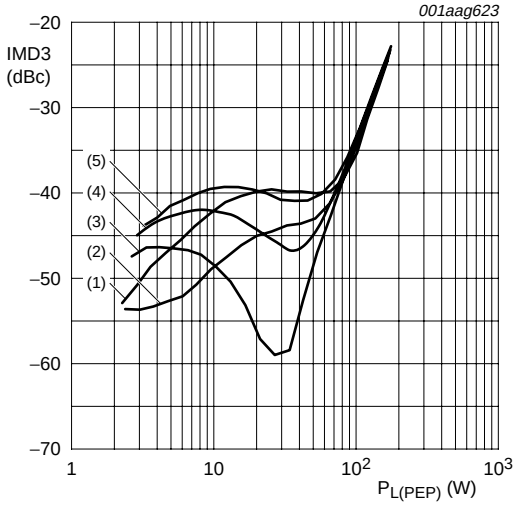
f	Z_S	Z_L
MHz	Ω	Ω
2110	1.9 – j2.8	1.7 – j1.8
2140	1.8 – j2.7	1.6 – j1.6
2170	1.7 – j2.6	1.5 – j1.4



(1) I_{Dq} = 850 mA
(2) I_{Dq} = 975 mA
(3) I_{Dq} = 1150 mA
(4) I_{Dq} = 1350 mA
(5) I_{Dq} = 1550 mA

V_{DS} = 28 V; f_1 = 2140.0 MHz; f_2 = 2140.1 MHz.

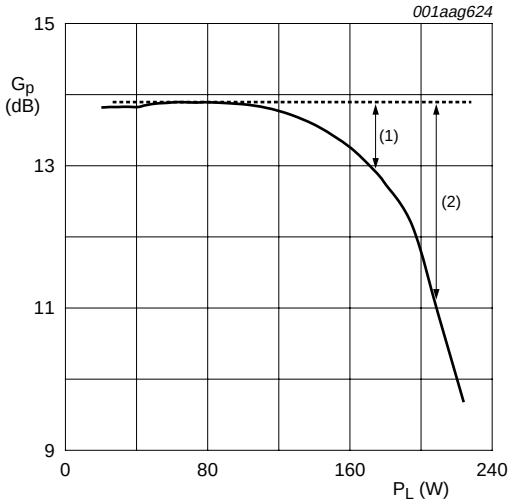
Fig 3. Two-tone power gain as a function of peak envelope load power; typical values



(1) I_{Dq} = 850 mA
(2) I_{Dq} = 975 mA
(3) I_{Dq} = 1150 mA
(4) I_{Dq} = 1350 mA
(5) I_{Dq} = 1550 mA

V_{DS} = 28 V; f_1 = 2140.0 MHz; f_2 = 2140.1 MHz.

Fig 4. Third order intermodulation distortion as a function of peak envelope load power; typical values



t_{on} = 8 µs; t_{off} = 1 ms.

(1) $P_{L(1dB)}$ = 174 W (= 52.4 dBm)
(2) $P_{L(3db)}$ = 209 W (= 53.2 dBm)

Fig 5. Pulsed peak power capability; typical values

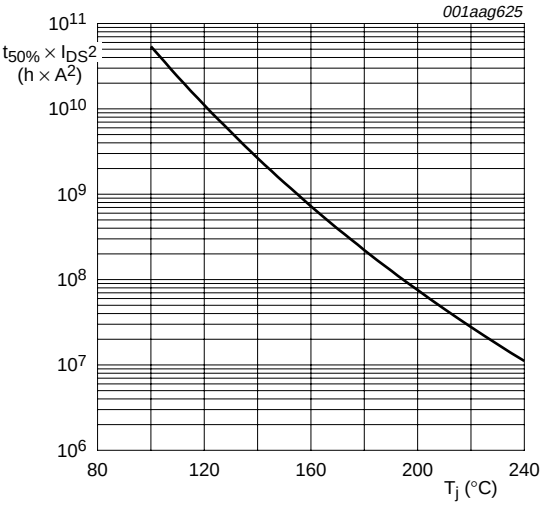
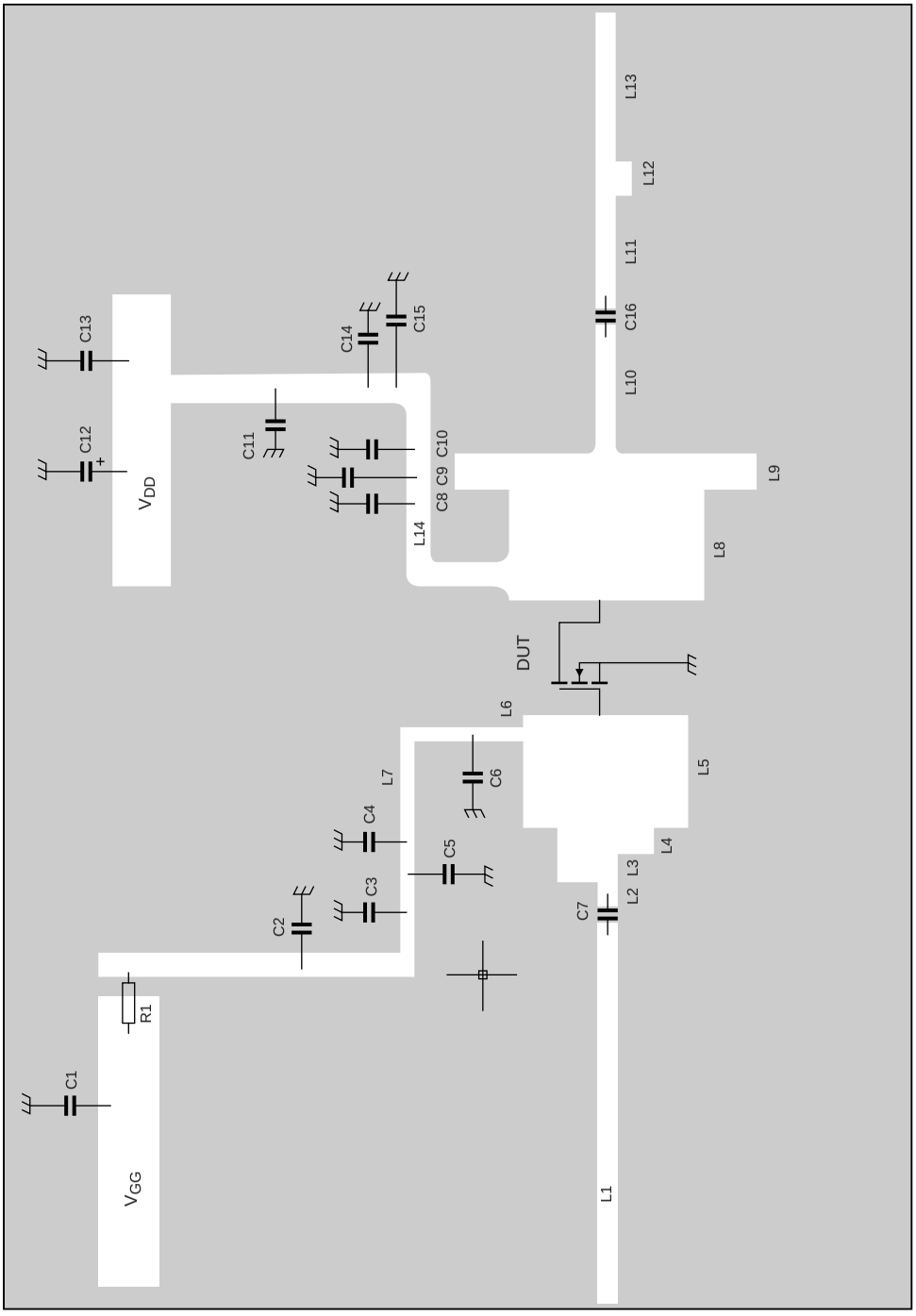


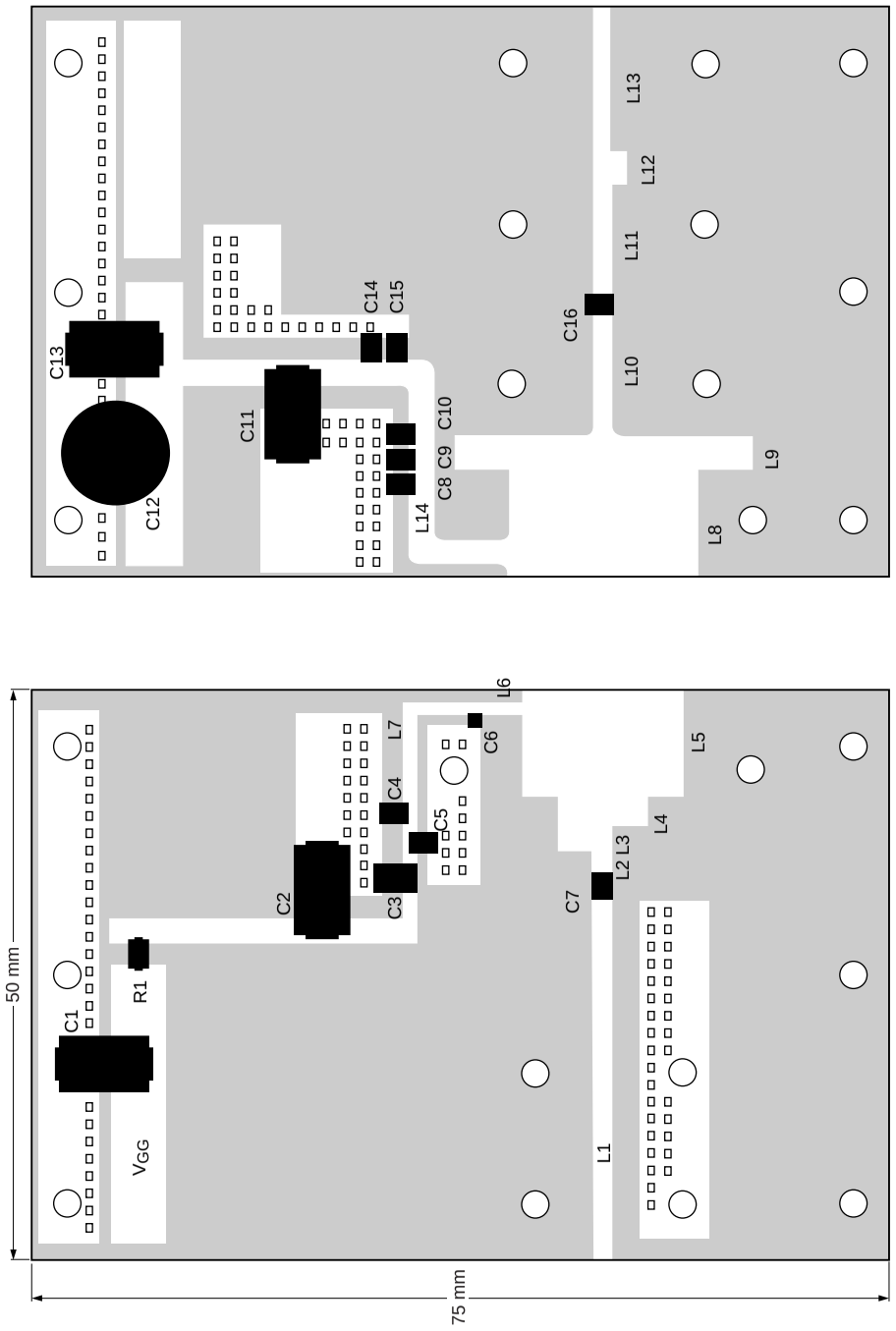
Fig 6. Time in hours to 50 % cumulative failure ($t_{50\%}$) due to electromigration as function of junction temperature

8. Test information



See Table 9 for list of components.

Fig 7. Schematic test circuit for operation at 2.14 GHz



The components are situated on a double copper-clad Taconic RF35 Printed-Circuit Board (PCB) (ε_r = 3.5); thickness = 0.76 mm. The other side is unetched and serves as a ground plane.

See Table 9 for list of components.

Fig 8. Component layout for 2.14 GHz test circuit

Table 9. List of components (see Figure 7 and Figure 8)

Component	Description	Value		Remarks
C1, C2, C11	tantalum capacitor	10 μF; 35 V		
C3	multilayer ceramic chip capacitor	4.7 μF; 25 V		
C4, C10	multilayer ceramic chip capacitor	8.2 pF	[2]	
C5, C8, C14, C15	multilayer ceramic chip capacitor	1.5 μF; 50 V		
C6	multilayer ceramic chip capacitor	0.6 pF	[1]	
C7	multilayer ceramic chip capacitor	4.7 pF	[2]	
C9	multilayer ceramic chip capacitor	220 nF; 50 V		
C12	electrolytic capacitor	220 μF; 63 V		
C13	tantalum capacitor	4.7 μF; 50 V		
C16	multilayer ceramic chip capacitor	7.5 pF	[1]	ATC180R
L1	stripline	Z_0 = 50 Ω	[3]	(W × L) 32.3 mm × 1.7 mm
L2	stripline	Z_0 = 50 Ω	[3]	(W × L) 2.2 mm × 1.7 mm
L3	stripline	Z_0 = 24 Ω	[3]	(W × L) 2.3 mm × 4.8 mm
L4	stripline	Z_0 = 15 Ω	[3]	(W × L) 2.4 mm × 8 mm
L5	stripline	Z_0 = 9.5 Ω	[3]	(W × L) 9.3 mm × 14 mm
L6	stripline	Z_0 = 60 Ω	[3]	(W × L) 4 mm × 1.2 mm
L7	stripline	Z_0 = 60 Ω	[3]	(W × L) 14.5 mm × 1.2 mm
L8	stripline	Z_0 = 8.2 Ω	[3]	(W × L) 9.3 mm × 16.8 mm
L9	stripline	Z_0 = 5.5 Ω	[3]	(W × L) 3 mm × 25.8 mm
L10	stripline	Z_0 = 50 Ω	[3]	(W × L) 11 mm × 1.7 mm
L11	stripline	Z_0 = 50 Ω	[3]	(W × L) 9.5 mm × 1.7 mm
L12	stripline	Z_0 = 34 Ω	[3]	(W × L) 3 mm × 3 mm
L13	stripline	Z_0 = 50 Ω	[3]	(W × L) 12.7 mm × 1.7 mm
L14	stripline	Z_0 = 43 Ω	[3]	(W × L) 13.5 mm × 2.1 mm
R1	SMD resistor	4.7 Ω; 0.1 W		

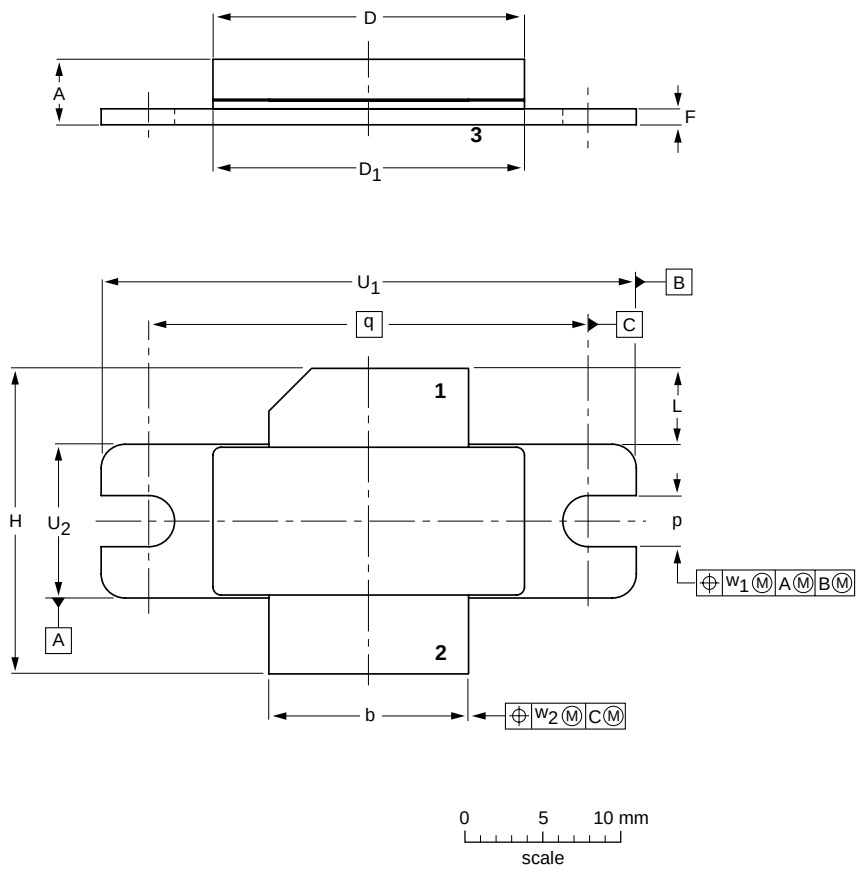
[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] Striplines are on a double copper-clad Taconic RF35 Printed-Circuit Board (PCB) (ε_r = 3.5); thickness = 0.76 mm.

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**



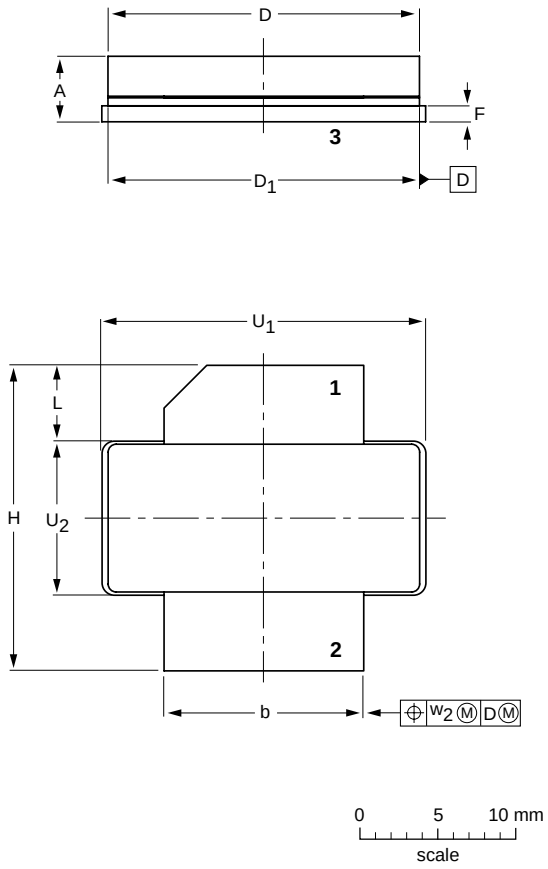
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~99-12-28~~ 03-01-10

Fig 9. Package outline SOT502A

Earless flanged LDMOST ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~03-01-10~~ 07-05-09

Fig 10. Package outline SOT502B

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
ACPR	Adjacent Channel Power Ratio
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
EDGE	Enhanced Data rates for GSM Evolution
EVM	Error Vector Magnitude
GSM	Global System for Mobile communications
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF4G22-130_4G22LS-130_1	20070703	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 3 July 2007

Document identifier: BLF4G22-130_4G22LS-130_1