Never stop thinking

TC1798

AP32164

Design Guideline for TC1798 Microcontroller Board Layout

Application Note

V1.2 2012-02

Microcontrollers

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Device1

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Page	Subjects (major changes since last revision)
10	Fig.4 changed.

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1 Overview

The TC1798 is a 32-Bit microcontroller in a BGA-516 package, which requires a PCB carefully designed for electromagnetic compatibility. In addition to the Infineon PCB Design Guidelines for Microcontrollers (AP24026), which gives general design rule informations for PCB design, some product-specific recommendations and guidelines for the TC1798 are discussed here.

1.1 General Information

The microcontroller has four supply domains (VDD=1.3V for Core, VDDP=3.3V for I/O Pad, VDDEBU=2.5V-3.3V for EBU, VDDM=3.3V or 5V for ADC), which should be decoupled individually.

The power supply feeding from the regulator outputs to each domain can be made on a supply layer (POWER).

1.2 Pinout of TC1798

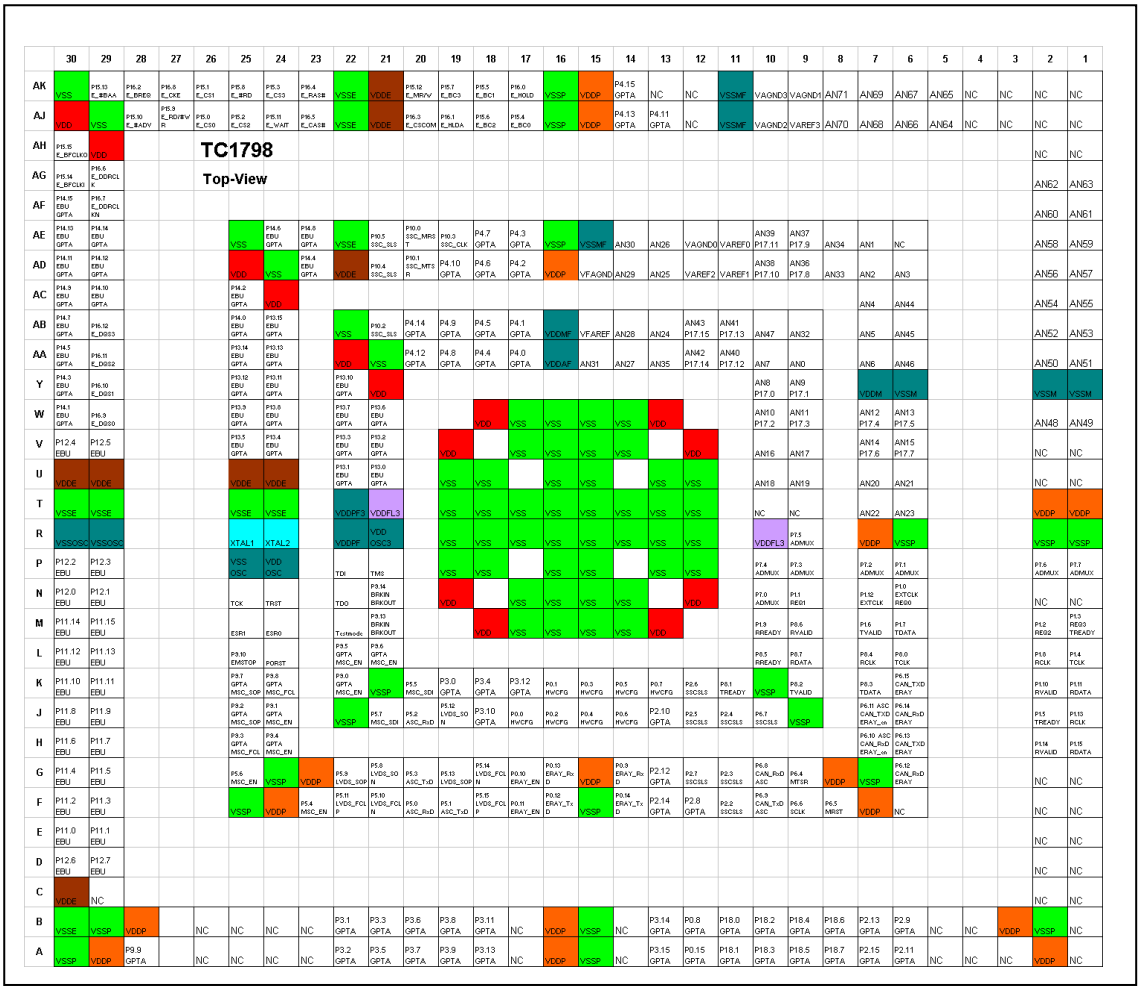

Figure 1 Pinout of TC1798 (BGA-516):

2 PCB Design Recommendations

- To minimize the EMI radiation on the PCB the following signals have to be considered as critical:
  - BFCLKOUT: EBU clock output
  - LVDS Pins

- MLI Pins
- MSC Pins
- ERAY Pins
- Supply Pins

Route these signals with adjacent ground reference and avoid signal and reference layer changes.

Route them as short as possible.

Routing ground on each side can help to reduce coupling to other signals.

- For unused **"Output, Supply, Input and I/O "** pins following points must be considered:

1. Supply Pins (Modules)	• See the User´s Manual.
2. I/O-Pins	• Should be configured as output and driven to static low in the weakest driver mode in order to improve EMI behaviour. Confuguration of the I/O as input with pullup is also possible. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
3. Output Pins including LVDS	• Should be driven static in the weakest driver mode. • If static output level is not possible, the output driver should be disabled. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
4.Input Pins without internal pull device	• For pins with alternate function see product target specification to define the necessary logic level. • Should be connected with high-ohmic resistor to GND (range 10k – 1Meg) wherever possible. No impact on design is however expected if a direct connection to GND is made. • Groups of 8 pins can be used to reduce number of external pull-up/down devices (keep in mind leakage current).
5. Input Pins with internal pull device	• For pins with alternate function see product specification to define the necessary logic level • Should be configured as pull-down and should be activated static low (exception: if the User´s Manual requires high level for alternate functions). No impact on design is expected if static high level is activated. • Solderpad should not be connected to any other net (isolated PCB-pad only for soldering)

- The ground system must be designed as follows:

  - Separate analog and digital grounds.

  - The analog ground must be separated into two groups:

    1. Ground for OSC and PLL (VSSOSC for VDDOSC, VDDOSC3, VDDPF and VDDPF3) as common star point.

    2. Ground for ADC (VSSM for VDDM, VSSMF for VDDMF/VDDAF) as common star point.

- To reduce the radiation / coupling from the oscillator circuit, a separated ground island on the GND layer should be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground connections

of the load capacitors and VSSOSC should also be connected to this island. Traces for the load capacitors and Xtal should be as short as possible.

- The power distribution from the regulator to each power plane should be made over filters (see Figure 2).
- RC Filters can be inserted in the supply paths at the regulator output and at the branchings to other module supply pins like VDDOSC, VDDOSC3, VDDFL3, VDDPF, VDDPF3, VDDM, VDDMF, VDDAF (see Figure 2). Using inductance or ferrite beads (5 – 10 µH) instead of the resistors can improve the EME behaviour of the circuit and reduce the radiation up to ~10dBµV on the related supply net.
- OCDS must be disabled.
- Select weakest possible driver strengths and slew rates for all I/Os (see Scalable Pads AppNote AP32111).
- Use lowest possible frequency for SYSCLK.
- Avoid cutting the GND plane by via groups. A solid GND plane must be designed.

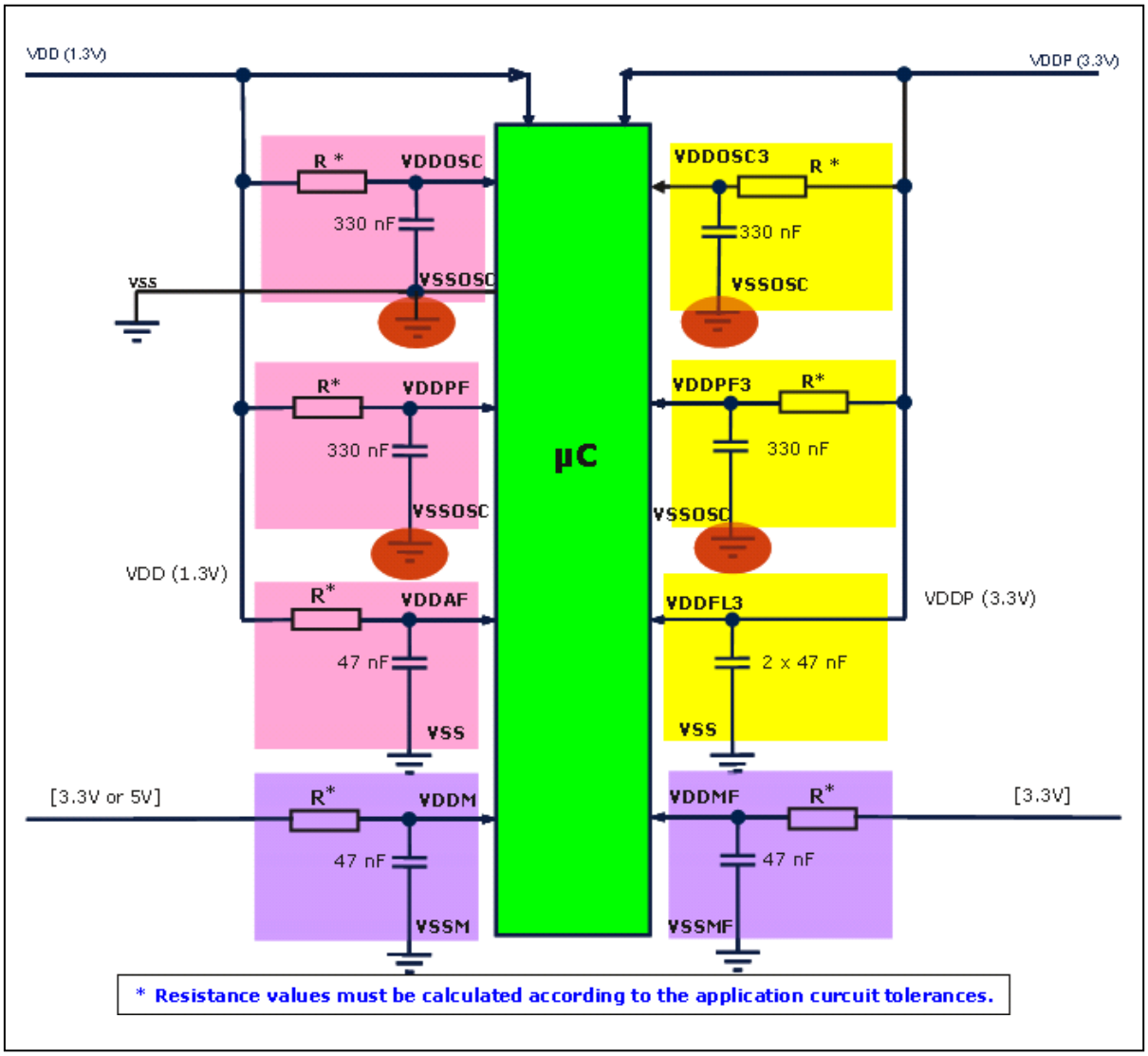

Figure 2 Filtering of VDDOSC, VDDOSC3, VDDFL3, VDDPF, VDDPF3, VDDM, VDDMF, VDDAF supply pins

2.1 Decoupling

- The three supply domains VDD, VDDP and VDDEBU of TC1798 should be decoupled separately (see decoupling placement example in Figure 3).
- Type of capacitors:
  - Values: 47 nF, 100 nF, 330 nF
  - X7R Ceramic Multilayer (low ESR and low ESL)
- All supply pins should be connected first to the dedicated decoupling capacitor and then from the capacitors over vias to the power planes.
- All VSS pins should be connected to the GND.
- The decoupling capacitors should be placed directly under the IC or if necessary, some capacitors can be placed on top layer close to the supply pins of the IC.
- Ground plane on bottom layer can be used to connect the capacitors. If no plane is used, they should be connected with vias to the GND layer.
- Multiple vias should be used at capacitors to get a low impedance connection between capacitors and POWER/GND planes or pins.
- All capacitors must be placed as close as possible to the related supply pin group.

In Figure 3 shown examples are based on device power supply concept and implementation. Alternative implementations are also acceptable and must be evaluated within application by customer.

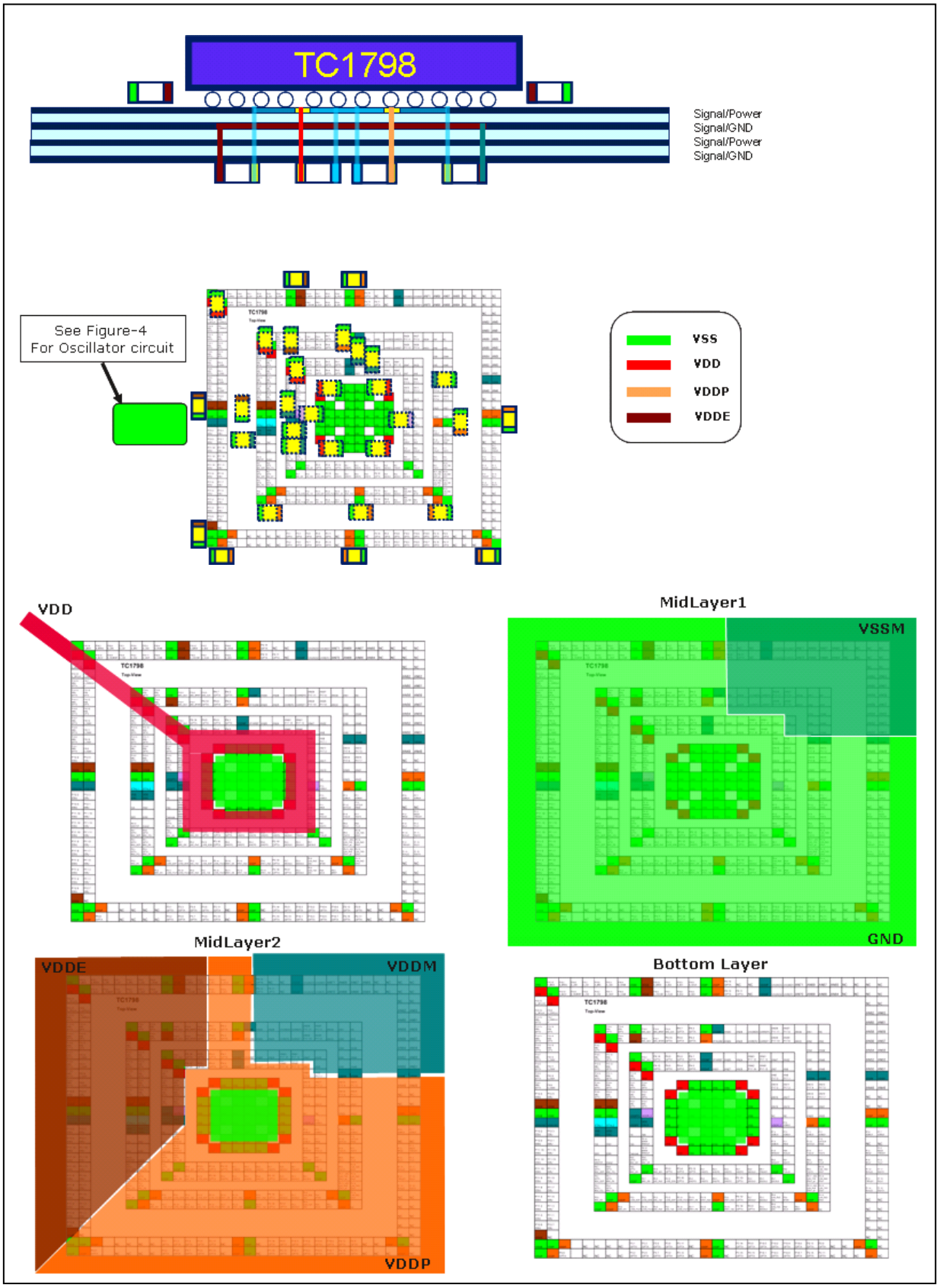

Figure 3 Capacitor Placement Example for Decoupling of TC1798 (BGA-516)

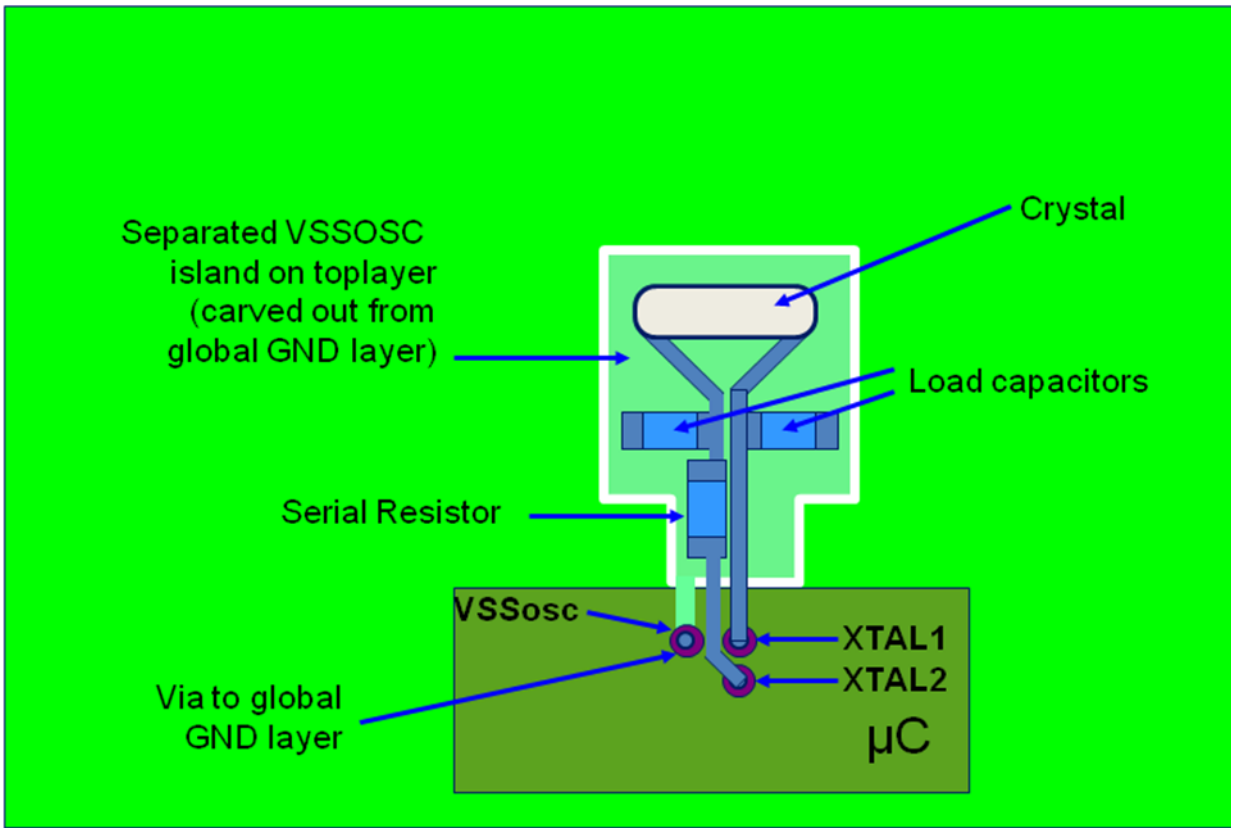

Figure 4 Layout Proposal Oscillator Circuit

2.2 Decoupling Capacitor List:

Capacitor	Supply	Pins(BGA-516)
47 nF	VDD center	M18/N19
47 nF	VDD center	M13/N12
47 nF	VDD center	V19/W18
47 nF	VDD center	V12/W13
47 nF	VDD entry row3	Y21/AA22
47 nF	VDD entry row2	AC24/AD25
47 nF	VDD entry row1	AH29/AJ30
47 nF	VDDSTBY (only emulation device)	T9/T10
47 nF	VDDP	A29/B28
47 nF	VDDP	A16/B16
47 nF	VDDP	A2/B3
47 nF	VDDP	F24/G23
47 nF	VDDP	G15
47 nF	VDDP	F7/G8
47 nF	VDDP	R7
47 nF	VDDP	T1/T2
47 nF	VDDP	AD16
47 nF	VDDP	AJ15/AK15
47 nF	VDDE	C30
47 nF	VDDE	U24/U25
47 nF	VDDE	U29/U30
47 nF	VDDE	AD22
47 nF	VDDE	AJ21/AK21
330 nF	VDDOSC	P24
330 nF	VDDOSC3	R21
47 nF	VDDFL3	R10
47 nF	VDDFL3	T21
330 nF	VDDPF	R22
330 nF	VDDPF3	T22
47 nF	VDDM	Y7
47 nF	VDDMF	AB16
47 nF	VDDAF	AA16
47 nF(optional 2,2µF)	VFAREF	AB15
47 nF(optional 2,2µF)	VAREF0	AE11
47 nF(optional 2,2µF)	VAREF1	AD11
47 nF(optional 2,2µF)	VAREF2	AD12
47nF(optional 2,2µF)	VAREF3	AJ9

Note: This application note contains design recommendations from Infineon Technologies point of view. Effectiveness and performance of the final application implementation must be validated by customer, based on dedicated implementation choices.

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