PIC12F635

PIC12F635
Silicon Errata and Data Sheet Clarification

The PIC12F635 devices that you have received conform functionally to the current Device Data Sheet (DS41232**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC12F635 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B3**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC12F635 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A1	B2	B3
PIC12F635	00 1111 101x xxxx	1	4	5

Note 1: The device and revision data is stored in the Device ID located at 2006h in program memory.

2: Refer to the *"PIC12F6XX/16F6XX Memory Programming Specification"* (DS41204) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions		
				A1	B2	B3
WDT	Prescaler	1.1	Spurious resets when modifying the prescaler assignment.	X		
WDT	Prescaler	1.2	Spurious resets when modifying the prescaler assignment.	X	X	X
EEPROM	EEIF Flag	2.	Flag inadvertently cleared.	X		
WUR	Wake-up Reset	3.	Power-up Timer not used on wake-up Reset.	X		
IESO	Clock Switching	4.	Processor may not wake if no external oscillator.	X		

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B3**).

1. Module: Resets

1.1 Resets (when WDT times out)

Modifying the settings of the shared Timer0 and Watch-dog Timer prescaler may cause device Resets. If the OPTION_REG bits: PS<2:0> are changed from any other value to '000', multiple spurious Resets can occur when the WDT times out. These Resets can occur even when the PSA bit is clear, assigning the prescaler to the Timer0.

Work around

If a CLRWDT instruction is issued before the WDT times out and before the OPTION register PS<2:0> bits are modified, this problem is eliminated.

Affected Silicon Revisions

A1	B2	B3					
X							

1.2 Timer0 and WDT Prescaler Assignment Spurious Reset

A Spurious Reset may occur if the Timer0/Watch-dog Timer (WDT) prescaler is assigned from the WDT to Timer0 and then back to the WDT.

Summary

The issue only arises when all of the below conditions are met:

- Timer0 external clock input (TOCKI) is enabled.
- The Prescaler is assigned to the WDT, then to the Timer0 and back to the WDT.
- During the assignments, the TOCKI pin is high when bit TOSE is set, or low when TOSE is clear.
- The 1:1 Prescaler option is chosen.

Description

On a POR, the Timer0/WDT prescaler is assigned to the WDT. If the prescaler is reassigned to Timer0 and Timer0 external clock input (TOCKI) is enabled, then the prescaler would be clocked by a transition on the TOCKI pin. On power-up, the TOCKI pin is (by default) enabled for Timer0 in the OPTION register.

If the TOCKI pin is:

- High and Timer0 is configured to transition on a falling edge (TOSE set), or
- Low and Timer0 is configured to transition on a rising edge (TOSE clear)

Then, if the prescaler is reassigned to the WDT, a clock pulse to the prescaler will be generated on the reassignment.

If the prescaler is configured for the 1:1 option, the clock pulse will incorrectly cause a WDT Time-out Reset of the device.

Work around

1. Disable the Timer0 external clock input by clearing the TOCKI bit in the OPTION register.
2. Modify the TOSE bit in the OPTION register to the opposite configuration for the logic level on the TOCKI pin.
3. Select a prescaler rate, other than 1:1, and issue a CLRWDT instruction before switching to the final prescaler rate.

Affected Silicon Revisions

A1	B2	B3					
X	X	X					

2. Module: Data EEPROM Memory

The EEIF flag may be cleared inadvertently when performing operations on the PIR1 register, simultaneously with the completion of a data EEPROM write. This condition occurs when the data EEPROM write timer completes at the same moment that the PIR1 register operation is executed. Register operations are those that have the PIR1 register as the destination and include, but are not limited to, BSF, BCF, ANDWF, IORWF and XORWF.

Work around

1. Avoid operations on the PIR1 register when writing to the data EEPROM memory.
2. Poll the WR bit (EECON1<1>) to determine when the write is complete.
3. Use a timer interrupt to catch any instances when the EEIF flag is inadvertently cleared. The timer interrupt should be set longer than 8 ms. If EEIF fails, then the timer interrupt occurs as a default time out. The WR and WRERR flags are checked as part of the timer Interrupt Service Routine to verify the data EEPROM write success.

4. If periodic interrupts are occurring in addition to the EEIF interrupts, then use a secondary flag to sense write completion. The secondary flag is set whenever data EEPROM writes are active. A data EEPROM write completion is indicated when the secondary flag is set and the WR flag is clear.

Affected Silicon Revisions

A1	B2	B3					
X							

3. Module: Wake-up Reset (WUR)

If a Wake-up Reset occurs when the Wake-up Reset (WURE) and Power-up Timer (PWTRE) Configuration bits are enabled, then there will not be a 72 ms time delay from the Power-up Timer, as expected.

Work around

None.

Affected Silicon Revisions

A1	B2	B3					
X							

4. Module: Internal/External Clock Switch Over (IESO)

If a Wake-up Reset occurs when the Wake-up Reset (WURE) and Internal/External Clock Switch Over (IESO) Configuration bits are enabled and there is no external clock applied to the chip when in the XT/HS configurations, the processor will remain in Reset and not begin executing instructions.

Work around

There is no work around for revision A silicon for this errata. However, this issue was corrected for revision B silicon. If a Wake-up Reset occurs when the Wake-up Reset and Internal/External Clock Switch Over Configuration bits are enabled in revision B silicon and Wake-up Reset occurs, the chip will wake up and reset as expected.

Affected Silicon Revisions

A1	B2	B3					
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41232**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (8/2004)
Issue 1 – When OPTION_REG bits, PS<2:0>, are clear, multiple spurious Resets can occur when the WDT times out.

Added Clarification/Corrections to the Data Sheet, Issues 1, 2 and 3 (changed to 8-pin MF **saw singulated** packaging).

Rev B Document (11/2004)

Added Module 2, “Data EEPROM Memory” for PIC12F635 silicon.

Rev C Document (01/2005)

Revised Modules 1 and 2.

Deleted Clarifications/Corrections to the Data Sheet. Data Sheet has been updated.

Rev D Document (07/2005)

Data Sheet Clarifications/Corrections Section: Added Module 1: New 4x4 DFN Package added.

Rev E Document (10/2005)

Data Sheet Clarifications/Corrections Section: Replaced 8-Lead Plastic Dual Flat No Lead Package 4x4 (DFN).

Rev F Document (02/2006)

Data Sheet Clarifications/Corrections section: Added Module 2: I/O Pins.

Rev G Document (03/2006)

Data Sheet Clarifications/Corrections section: Added Module 3: Data EEPROM Memory; Added Module 4: Electrical Specifications.

Rev H Document (06/14/06)

Added Module 3: “Wake-up Reset”, and Module 4: “Internal/External Clock Switch Over”.

Rev J Document (04/2007)

Data Sheet Clarifications/Corrections section: Removed Data Sheet Modules per data sheet update.

Rev K Document (09/2009)

Updated the errata to the new format; Added item 1.2, “Timer0 and WDT Prescaler Assignment Spurious Reset”; Deleted the “Date Codes” section; Added new paragraph to Module 1; Other minor corrections.

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