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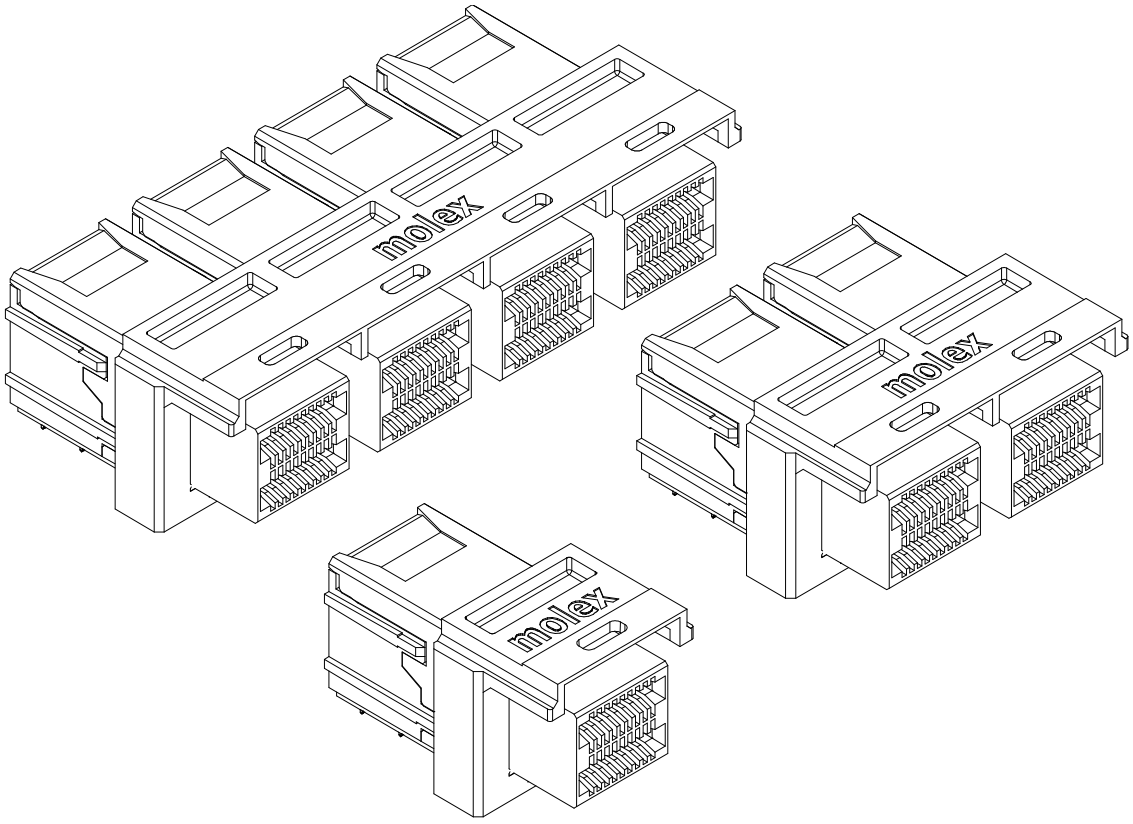
1.0 SCOPE

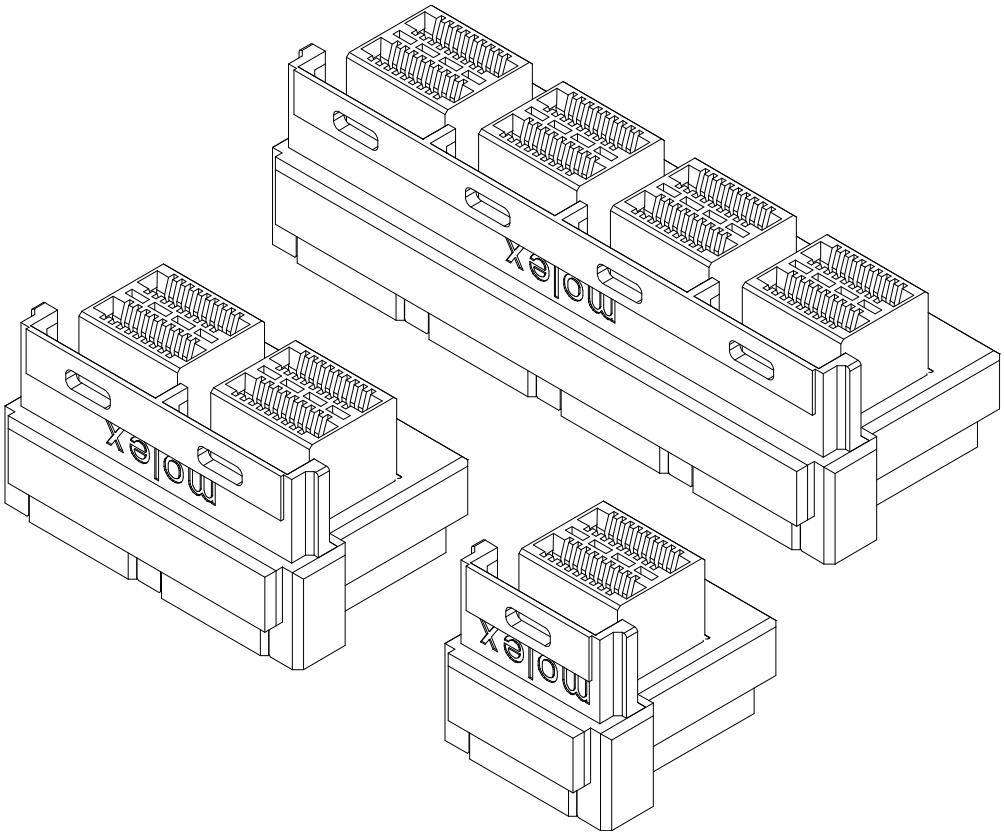
This specification covers the high speed PCB routing guidelines for the iPass HD (High Density) internal connector series. The connector has a single port with two card slot openings and is configured as 1X1, 1X2 and 1X4 assemblies. The connector compliant contact pins are press-fit mounted into a PC board with plated finished through holes.

Refer to product illustrations below.

Disclaimer: Molex does not guarantee the performance of the final product to the information provided in this document. All information in this report is considered Molex proprietary and confidential. This guide is not intended as a substitute for engineering analysis.



iPass+ HD Right Angle



iPass zHD Vertical

2.0 PRODUCT DESCRIPTION

The connector consists of housing with double 18-position receptacle ports and with compliant pin contacts on 0.75 centerline spacing. Each port has a card entry slot that accepts an integrated circuit card housed in the mating plug.

3.0 REFERENCE DOCUMENTS

Refer to the appropriate Sales Drawing for product part numbers.
Refer to PS-76867-001 for the connector Product Specification
Refer to AS-76867-001 & AS-170729-0001 for Application Specification
Refer to EE-76866-001 & EE-170729-0001 for Electrical Models

4.0 PC BOARD REQUIREMENTS

4.1 MATERIAL THICKNESS

The pc board material shall be glass epoxy (FR-4 or G-10). The recommended minimum pc board thickness shall be 1.57 mm.

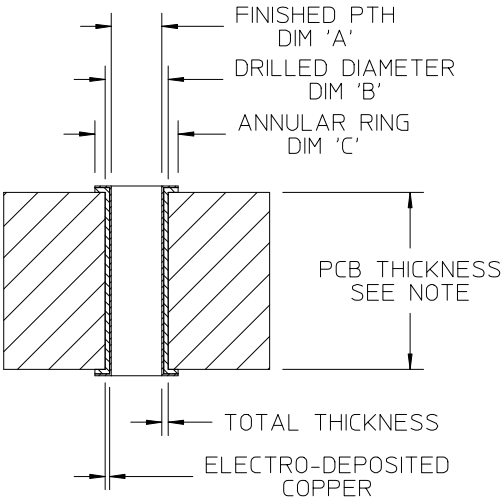
4.2 TOLERANCE

Maximum allowable bow of the pc board shall be 0.08 mm over the length of the connector assembly.

4.3 HOLE DIMENSIONS

The holes for the connector assembly must be plated through to dimensions specified in Figure 2.

Recommended Hole Dimensions



DIM. "A" MM / (INCH)	**DIM. "B"** MM / (INCH) - # DRILL	**DIM. "C"** MM / (INCH)
1.05+/-0.05 (.0413+/-.002)	1.181 (.0465) - # 56	1.40 (.055)
0.81+/-0.05 (.032+/-.002)	0.711 (.028) - # 70	1.16 (.046)
0.57+/-0.05 (.022+/-.002)	0.66 (.026) - # 71	0.91 (.036)
0.46+/-0.05 (.0181+/-.002)	0.572 (.022) - # 74	0.81 (.032)
0.37+/-0.05 (.0146+/-.002)	0.457 (.018) - # 77	0.72 (.028)

Note: Refer to appropriate sales drawing for recommended PCB holes and PCB thickness

PLATING DETAIL FOR COMPLIANT PIN HOLES
Figure 2

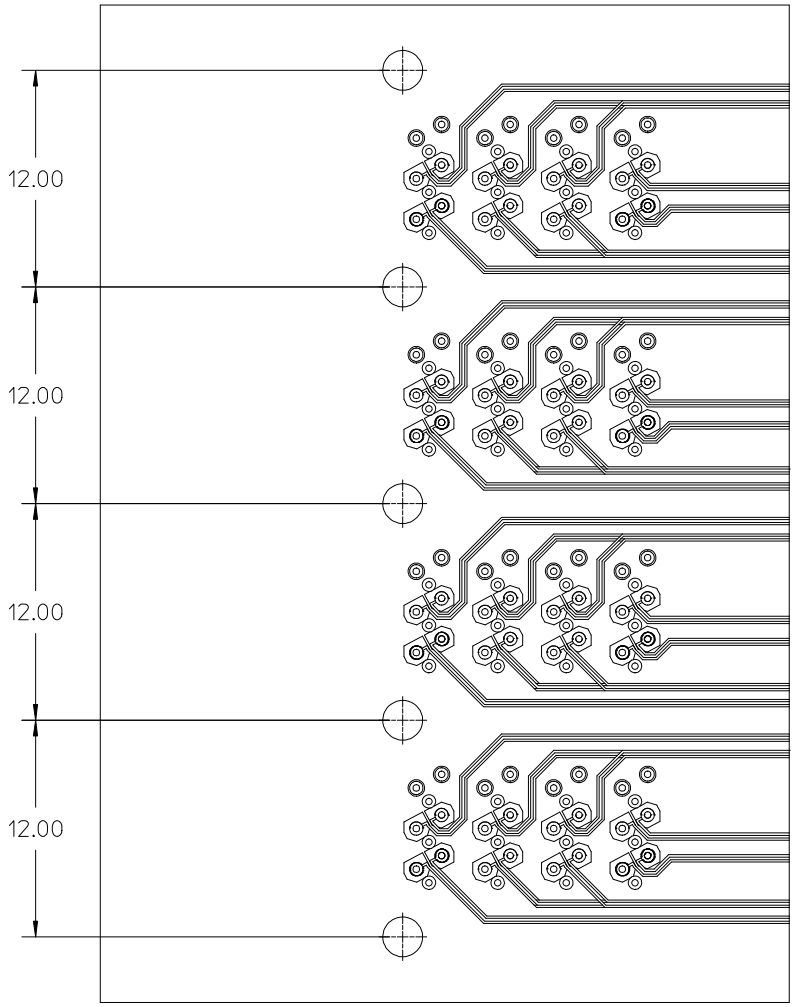
4.4 LAYOUT

The holes for the connector assembly must be precisely located to ensure proper placement and optimum performance of the connector assembly. Refer to the applicable Sales Drawing for the recommended hole pattern, dimensions, and tolerances.

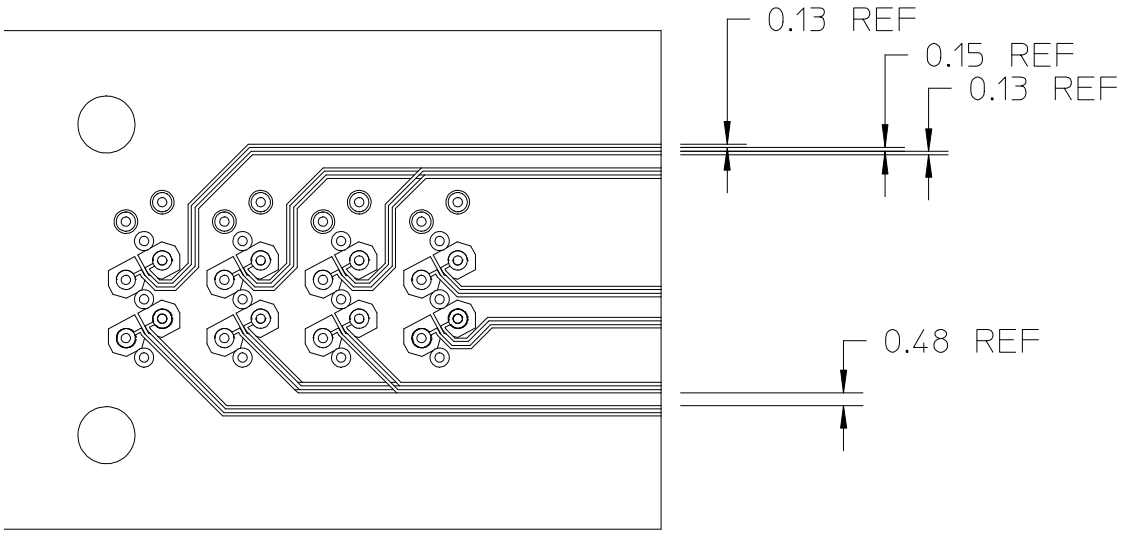
5.0 HIGH-SPEED ROUTING

5.1 6 GBPS APPLICATION

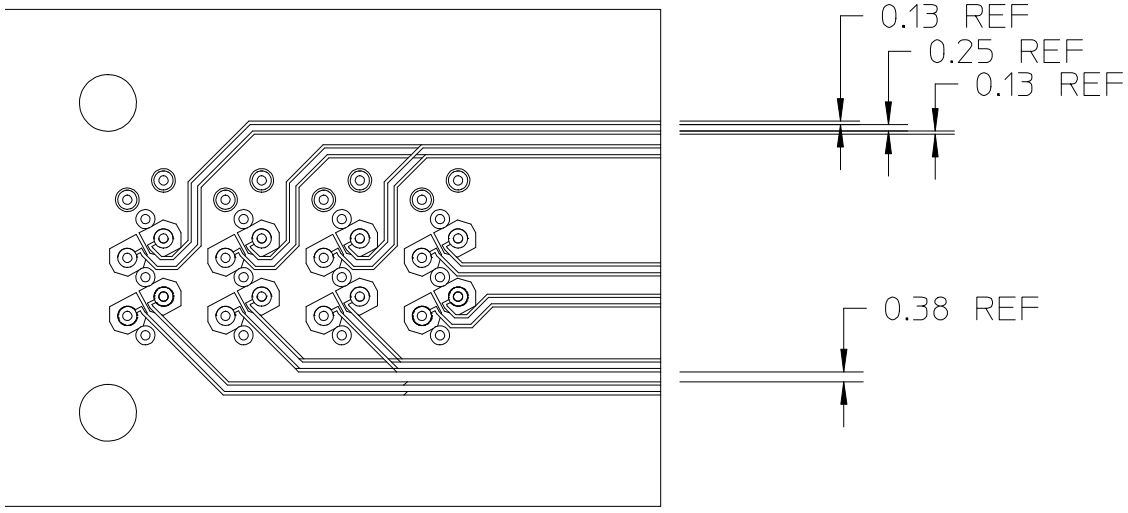
5.1.1 GENERAL ROUTING EXAMPLE (other configurations are possible)



Showing 3 layers overlaid for a typical side by side stacking (2 signal and ground layer)
Routing example shown for reference only
Shown with 0.13mm (0.005”) traces and 0.15mm (0.006”) spaces
0.48mm (0.019”) spaces between pair traces

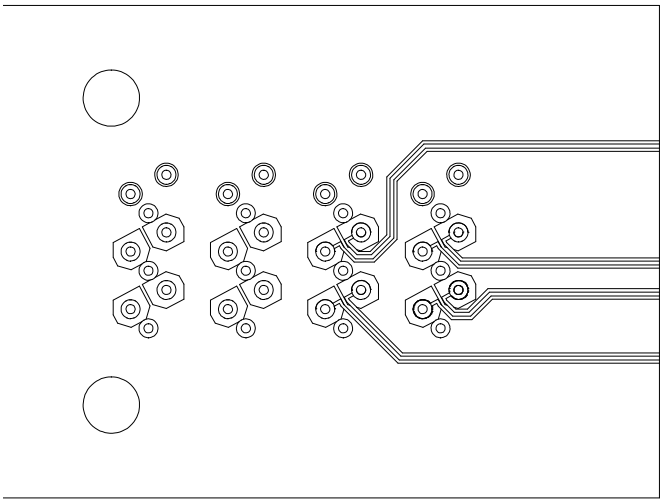


5-6-5 Routing

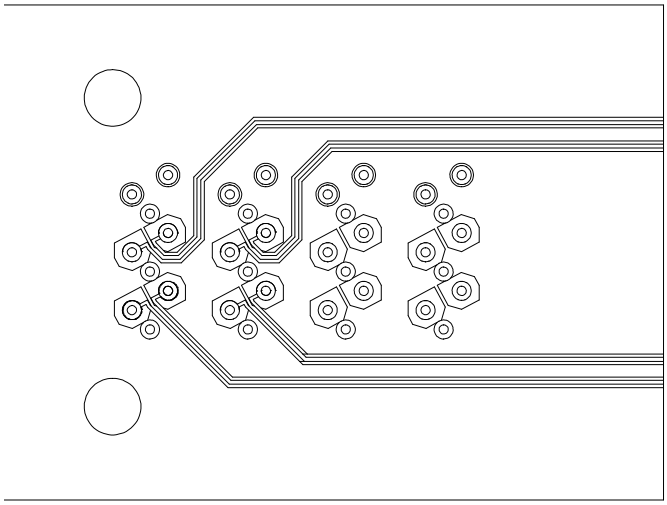


5-10-5 Routing

Showing 3 layer overlaid for a single connector (2 signal and ground layer)
Routing example shown for reference only
Shown with 0.13mm (0.005”) traces and 0.15mm (0.006”) spaces
0.48mm (0.019”) spaces between pair traces
and with 0.13mm (.005”) traces and 0.25mm (.010”) spaces
0.38mm (.015”) spaces between pair traces



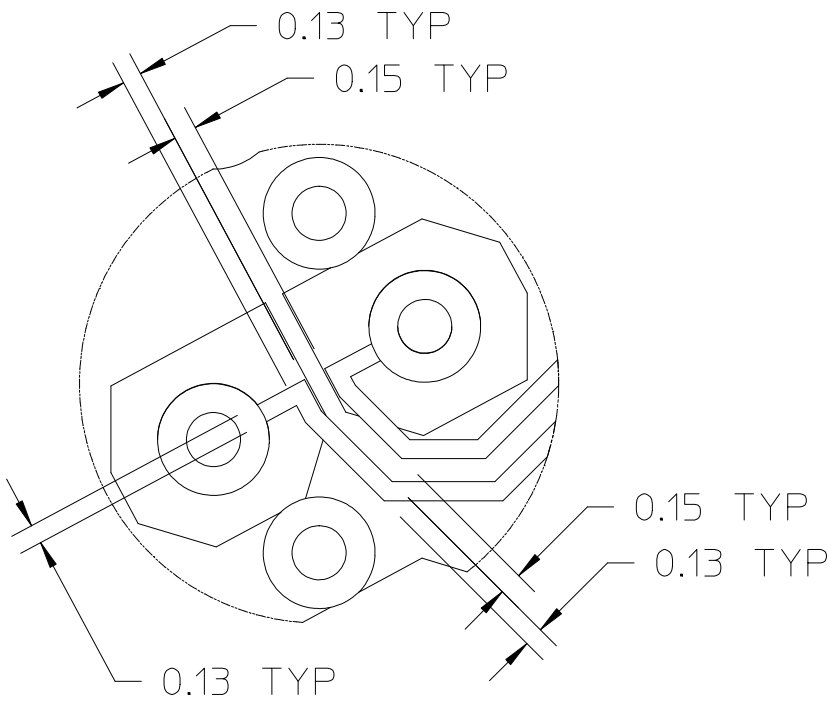
Board layer 1



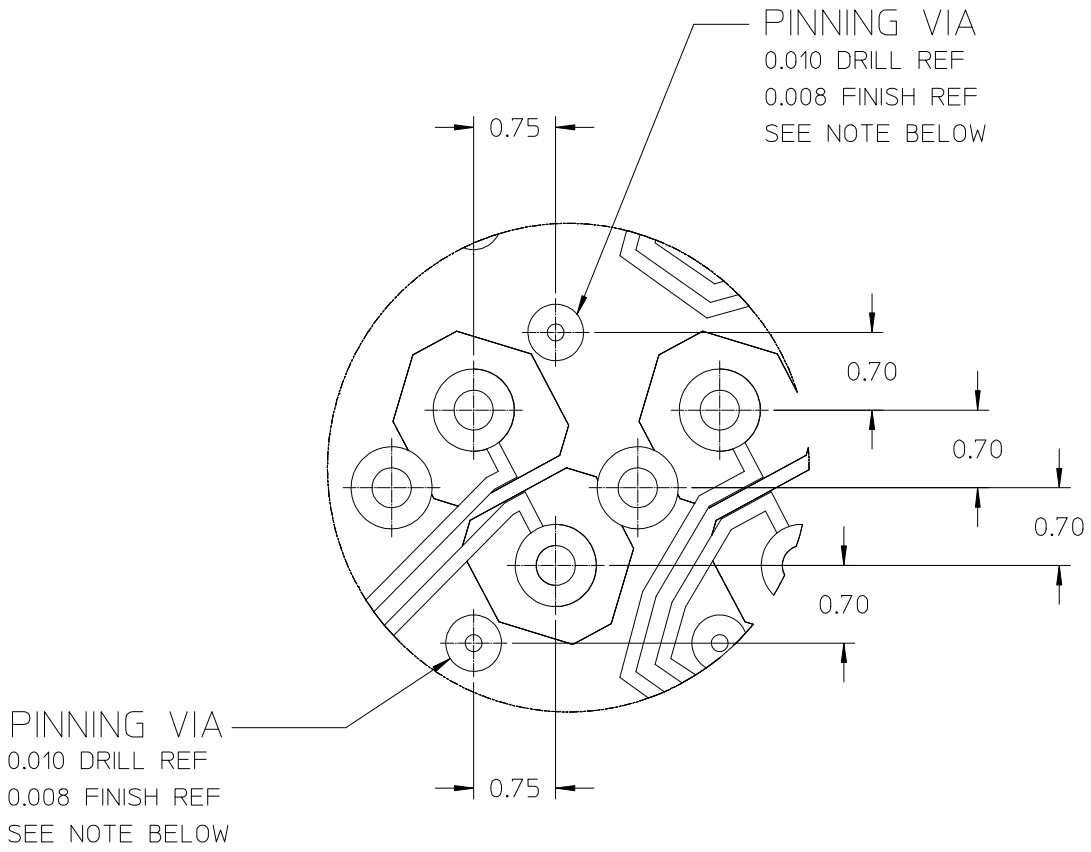
Board layer 2

5.1.2 HIGH-SPEED TRANSMISSION LINE PLANE

Ground layer shown reference with spacing between trace pairs
Routing example shown for reference only
Shown with 0.13mm (0.005") traces and 0.17mm (0.0065") spaces
0.75mm (0.0295") spaces between pair traces



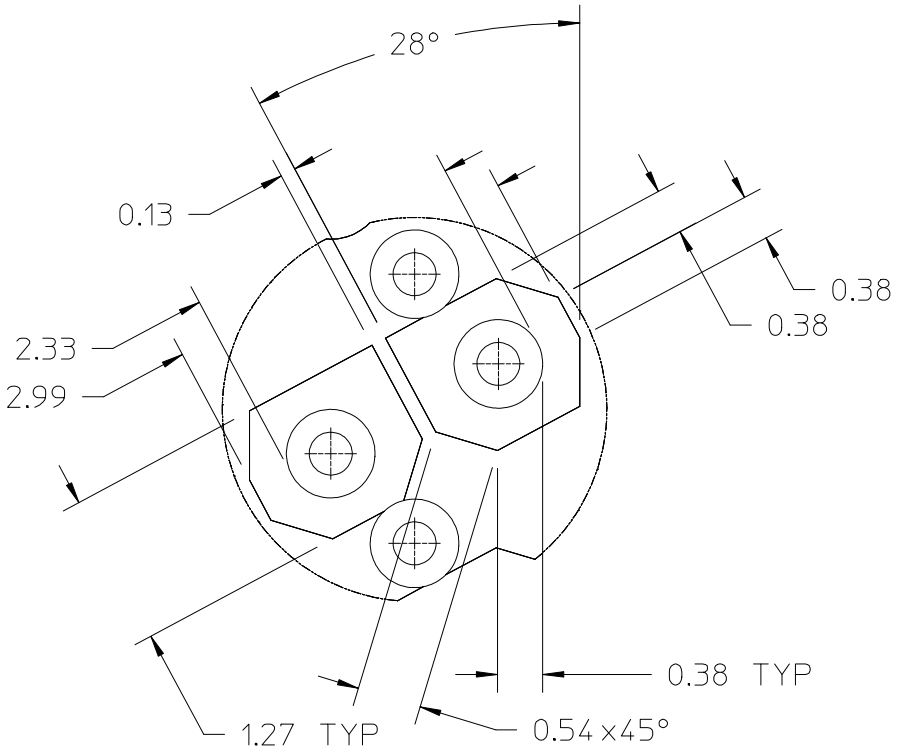
Trace detail typical for all trace positions



Note:
Option pinning VIA within connector footprint for additional electrical performance, location and size can vary from recommendation to meet board thickness, routing and electrical performance requirements.

5.1.3 HIGH-SPEED REFERENCE PLANE ANTI-PAD

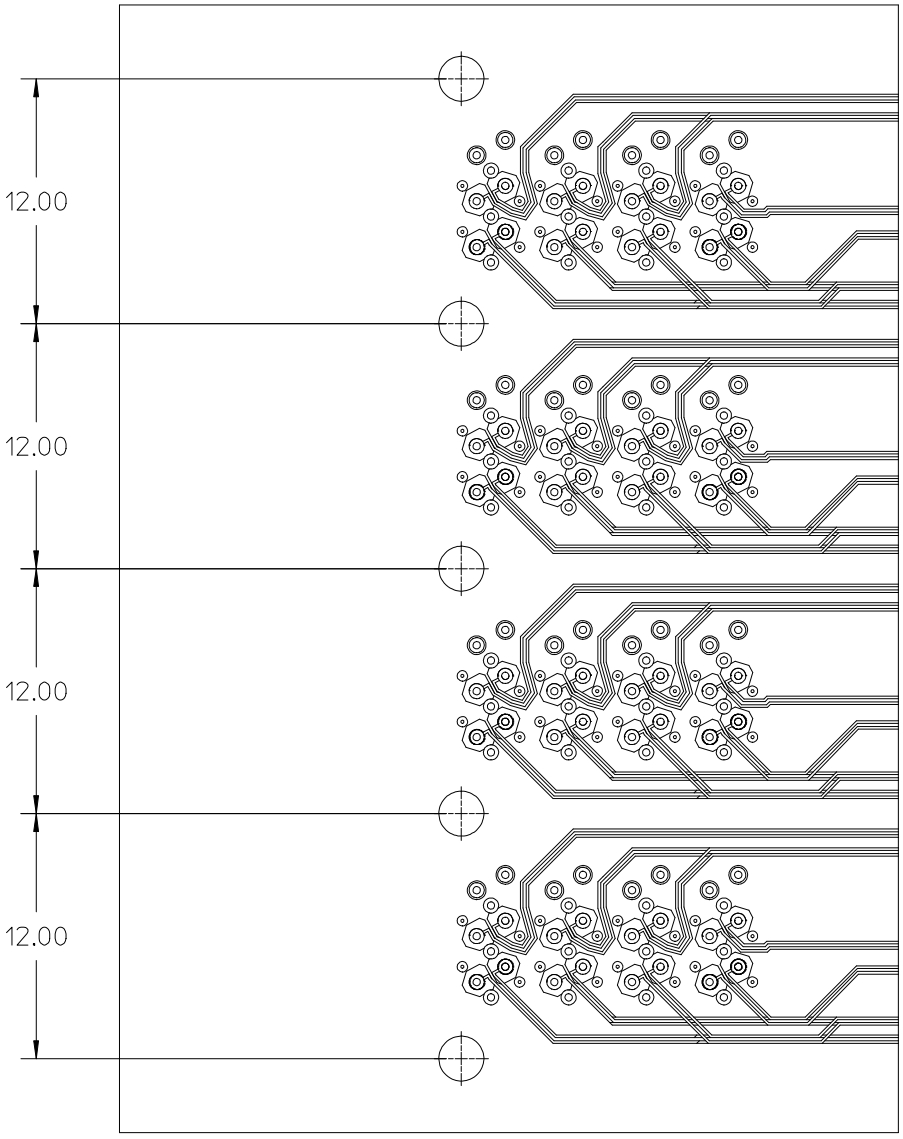
Signal Ground Planes



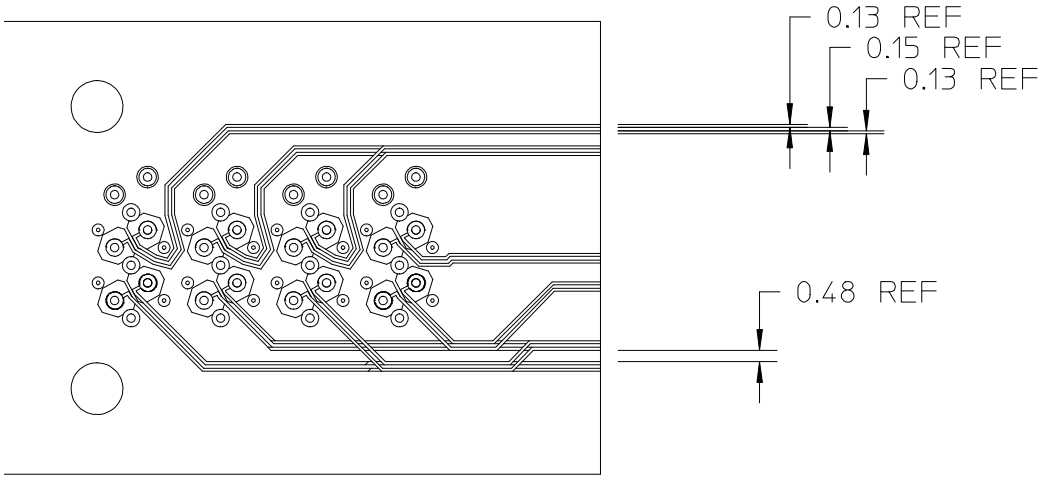
Chamfers may be eliminated, but must be done in a balanced fashion

5.2 12 GBPS APPLICATION

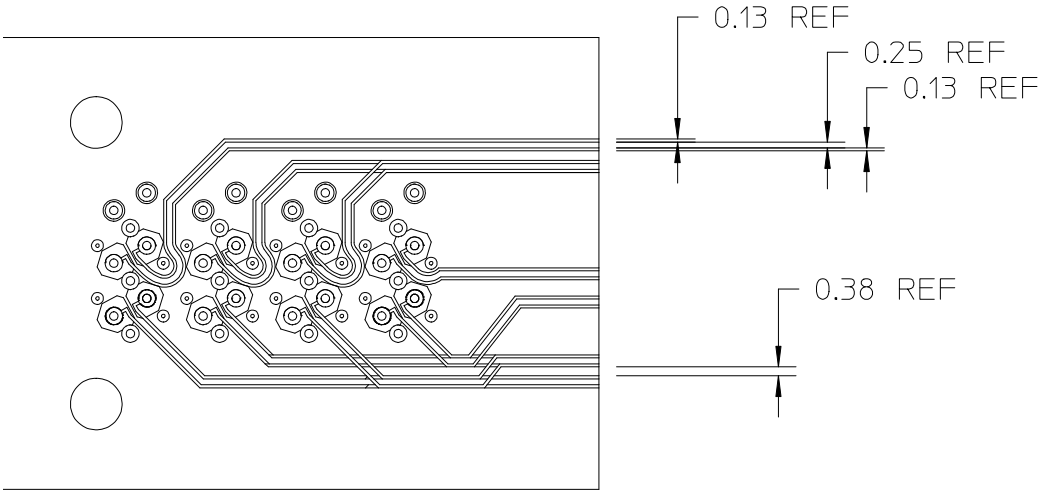
5.2.1 GENERAL ROUTING EXAMPLE (other configurations are possible)



Showing 3 layers overlaid for a typical side by side stacking (2 signal and ground layer)
Routing example shown for reference only
Shown with 0.13mm (0.005”) traces and 0.15mm (0.006”) spaces
0.48mm (0.019”) spaces between pair traces

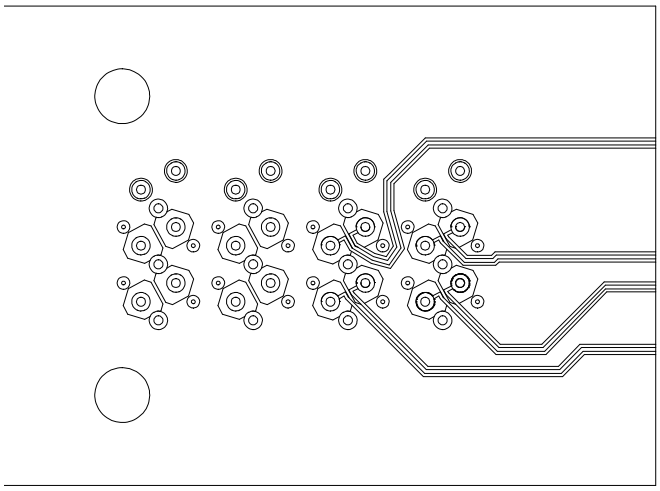


5-6-5 Routing



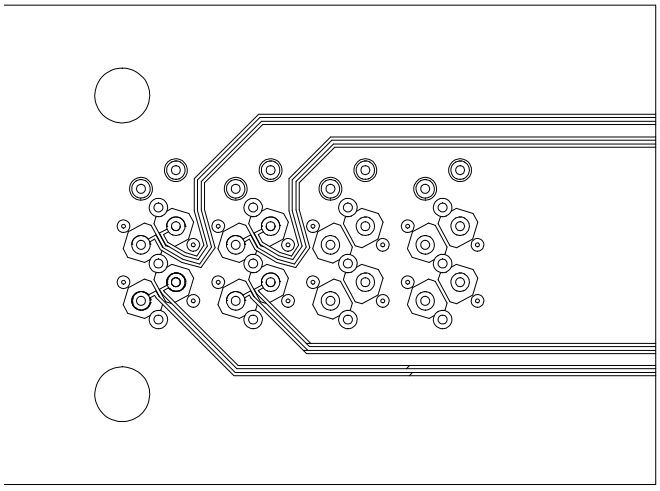
5-10-5 Routing

Showing 3 layer overlaid for a single connector (2 signal and ground layer)
Routing example shown for reference only
Shown with 0.13mm (.005”) traces and 0.15mm (.006”) spaces
0.48mm (.019”) spaces between pair traces
and with 0.13mm (.005”) traces and 0.25mm (.010”) spaces
0.38mm (.015”) spaces between pair traces



Differential Pair
Signal Layer 1

Board layer 1

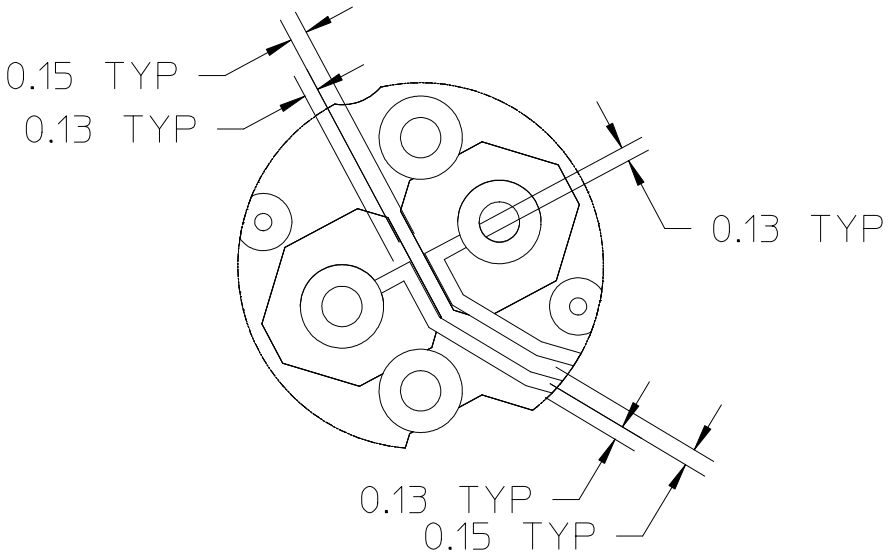


Differential Pair
Signal Layer 2

Board layer 2

5.2.2 HIGH-SPEED TRANSMISSION LINE PLANE

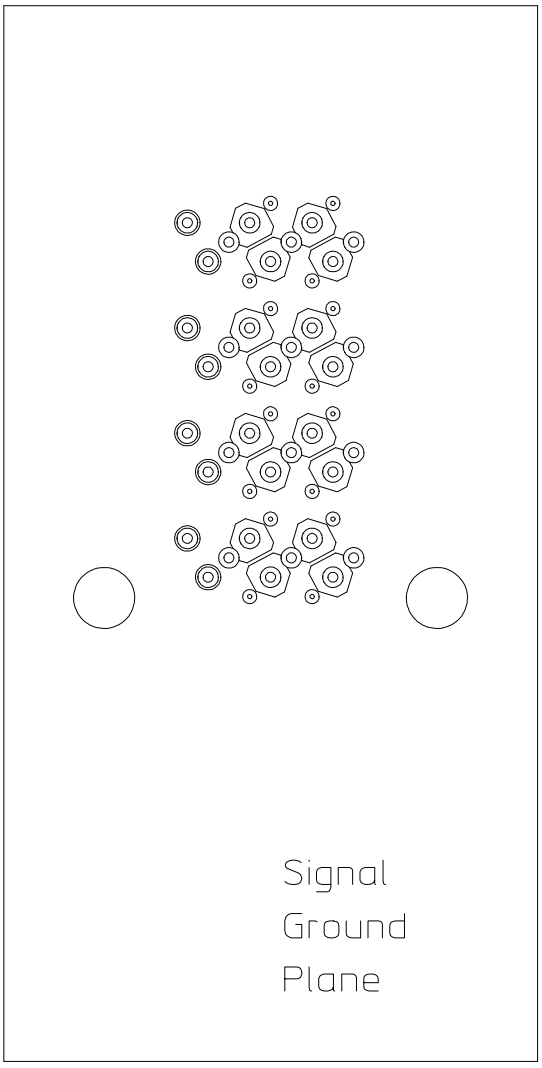
Ground layer shown reference with spacing between trace pairs
Routing example shown for reference only
Shown with 0.13mm (0.005") traces and 0.17mm (0.0065") spaces
0.75mm (0.0295") spaces between pair traces

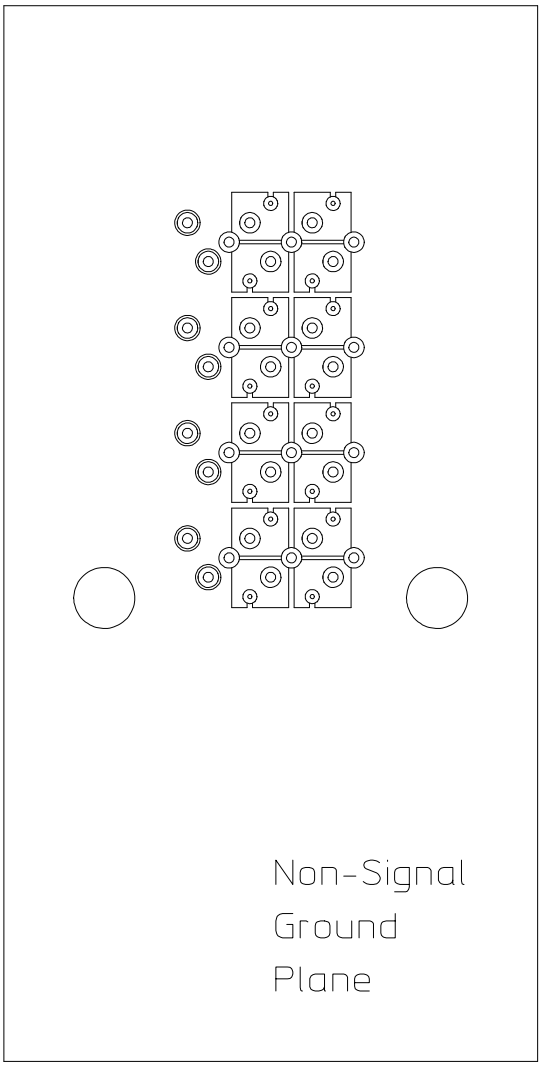


Trace detail typical for all trace positions

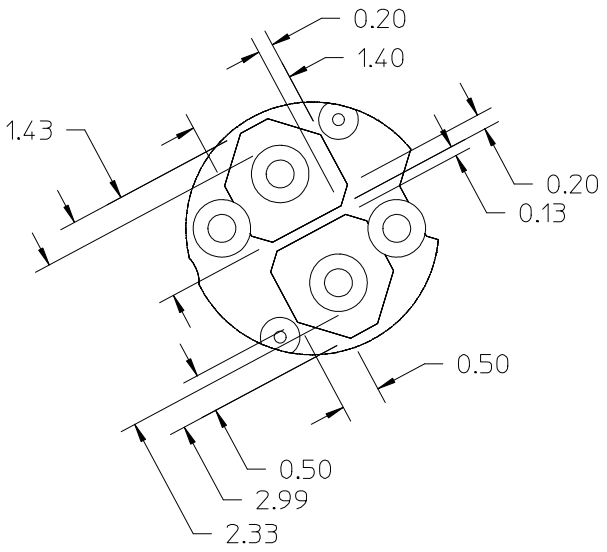
5.2.3 HIGH-SPEED TRANSMISSION LINE PLANE

Signal Ground Planes **Non-Signal Ground Planes**

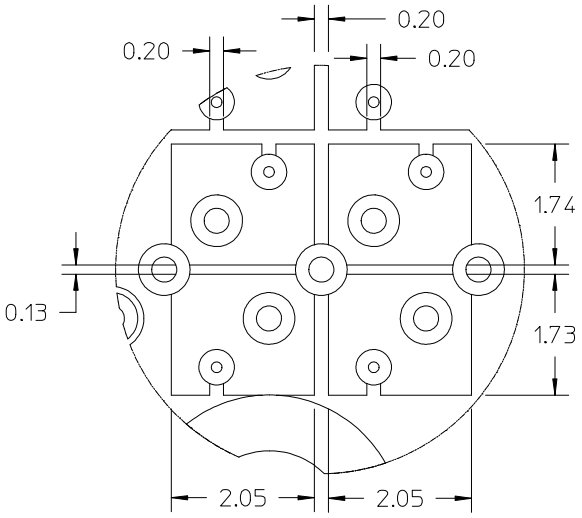




Signal Ground Planes

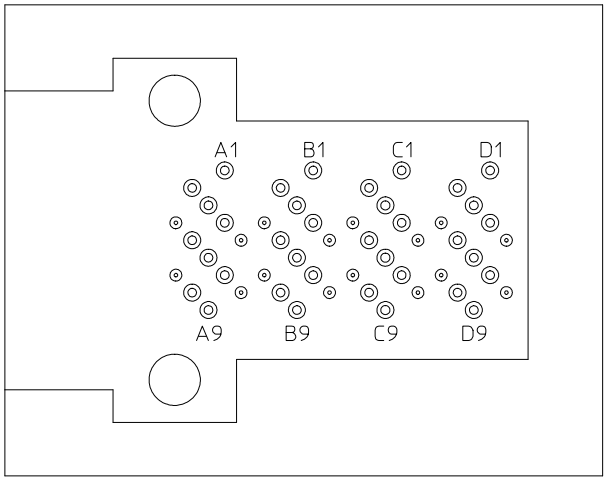


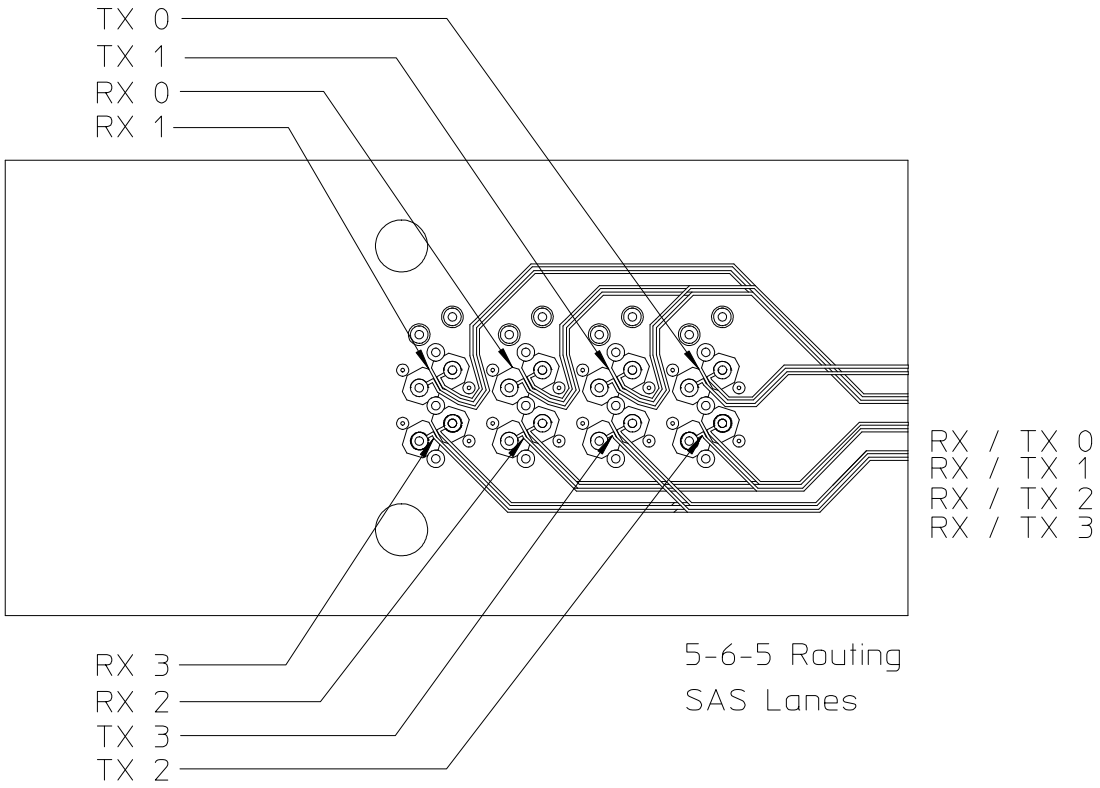
Non-Signal Ground Planes

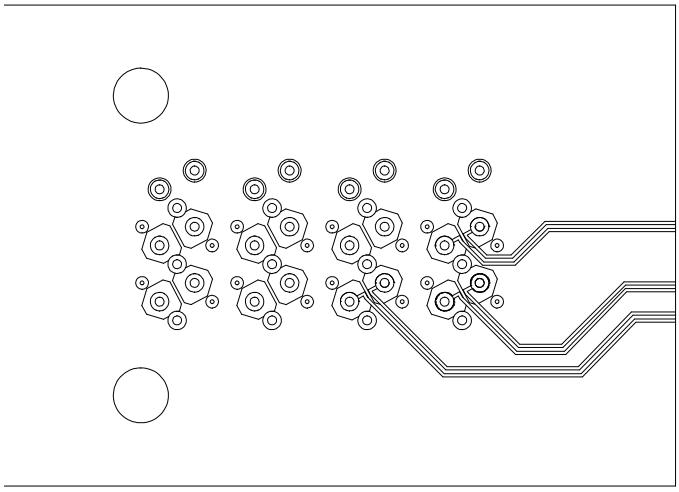


Chamfers may be eliminated, but must be done in a balanced fashion
Signal and Non-Signal features may be mixed on a layer

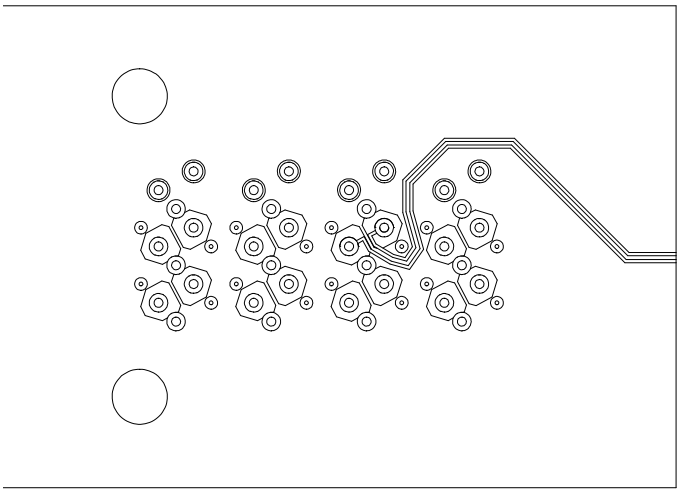
5.3 SAS LANE ROUTING EXAMPLE



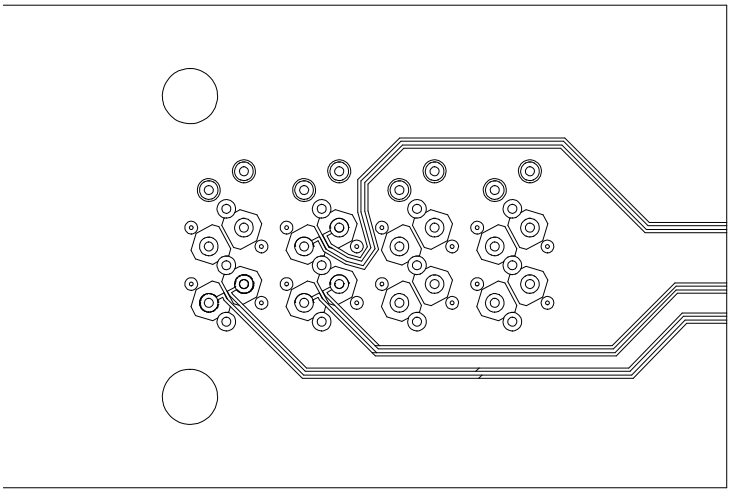




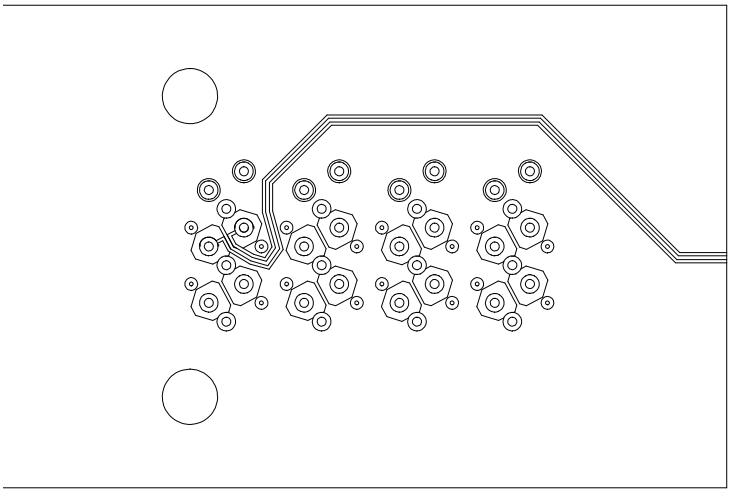
Differential Pair
Signal Layer 1



Differential Pair
Signal Layer 2

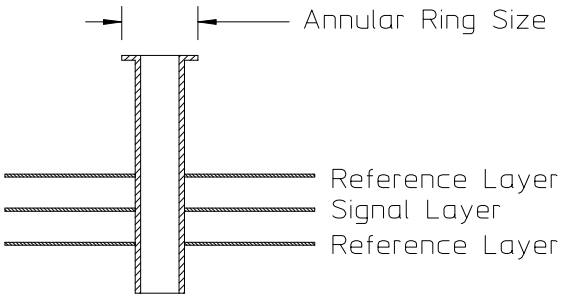


Differential Pair
Signal Layer 3

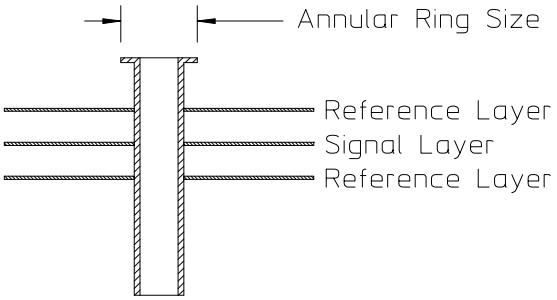


Differential Pair
Signal Layer 4

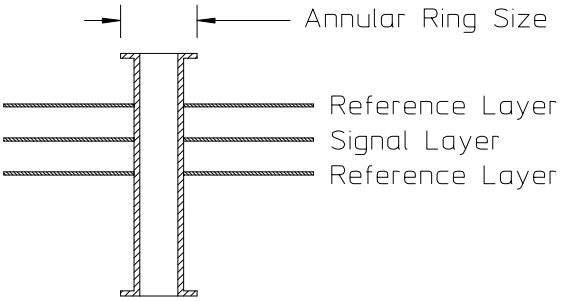
5.4 CONNECTOR PRESS-FIT INTERFACE VIA STUBS



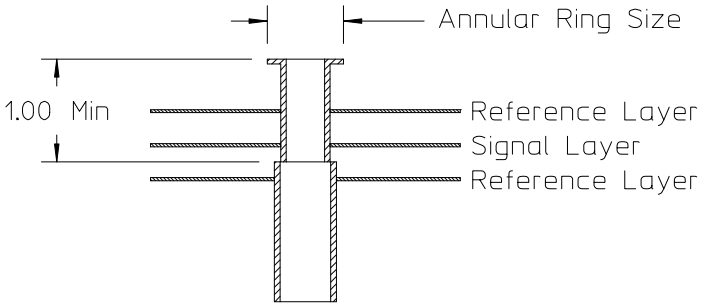
BOTTOM LAUNCH
DRIVEN VIA
(PREFERRED)



TOP LAUNCH
STUB VIA
(WORSE CASE)



STANDARD VIA CONFIGURATION



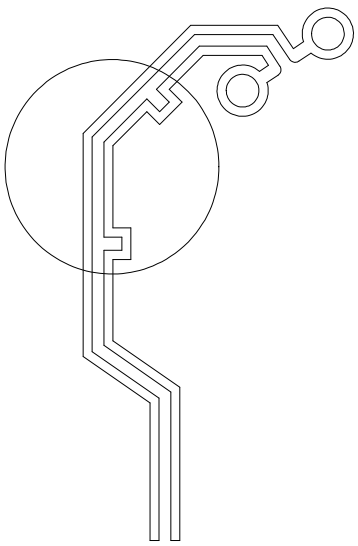
BACK DRILLED 1.00MM MAX FROM TOP

Only two annular rings are required for retention of the press-fit via within the printed circuit consequently annular rings on the bottom layer are not needed. Removing the bottom layer annular ring helps minimize the parasitic stub capacitance created by the via.

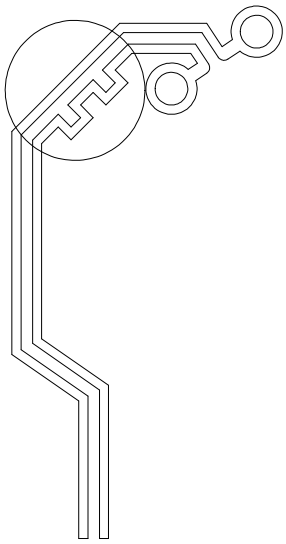
The anti-pad can be used on other ground layers not shown above. Alternatively, the anti-pad can be made larger with a broader keep-out region on these other ground layers to minimize parasitic capacitance.

For the connector press-fit vias, specify not only the 0.37mm (0.014") finished hole size but also the 0.45715mm (0.018") drill size for the board fabrication.

5.5 SKEW COMPENSATION



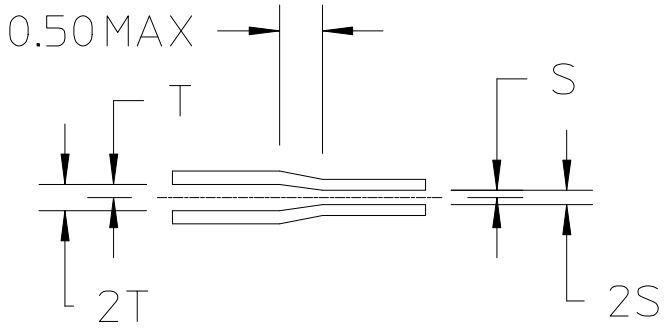
PREFERRED



NOT RECOMMENDED

It is recommended that skew compensation be distributed verses grouped in one or more locations.

5.6 TRACE COMPARISON



TRANSITION SHOULD BE SYMMETRIC

AM-76867-PCB-Routing.bdl