Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

July 2015

FDMT80080DC

N-Channel Dual Cool™ 88 PowerTrench® MOSFET

80 V, 254 A, 1.35 mΩ

Features

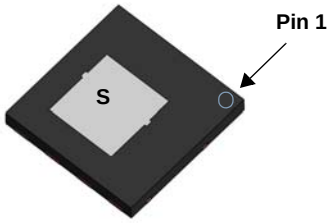
- Max $r_{DS(on)}$ = 1.35 mΩ at V_{GS} = 10 V, I_D = 36 A
- Max $r_{DS(on)}$ = 1.82 mΩ at V_{GS} = 8 V, I_D = 31 A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- Low profile 8x8mm MLP package
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

General Description

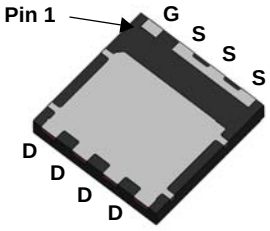
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process. Advancements in both silicon and Dual Cool™ package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

Applications

- OringFET / Load Switching
- Synchronous Rectification
- DC-DC Conversion

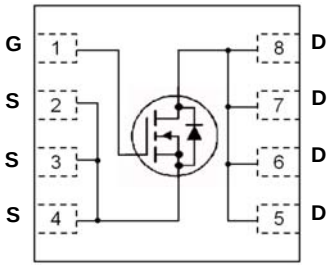


Top



Bottom

Dual Cool™ 88



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			80	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25 °C	(Note 5)	254	A
	-Continuous	T_C = 100 °C	(Note 5)	160	
	-Continuous	T_A = 25 °C	(Note 1a)	36	
	-Pulsed		(Note 4)	1453	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	1734	mJ
P_D	Power Dissipation	T_C = 25 °C		156	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	3.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Top Source)	1.6	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Bottom Drain)	0.8	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1k)	9	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
80080DC	FDMT80080DC	Dual Cool™ 88	13"	13.3 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted.

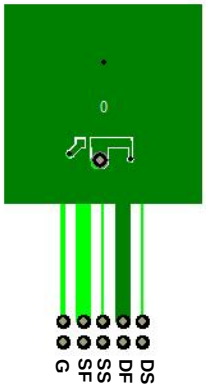
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		41		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-12		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 36 A		1.06	1.35	mΩ
		V_{GS} = 8 V, I_D = 31 A		1.23	1.82	
		V_{GS} = 10 V, I_D = 36 A, T_J = 125 °C		1.74	2.22	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 36 A		116		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		14800	20720	pF
C_{oss}	Output Capacitance			2080	2915	pF
C_{rss}	Reverse Transfer Capacitance			56	125	pF
R_g	Gate Resistance		0.1	1.8	4.5	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 40 V, I_D = 36 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		67	108	ns
t_r	Rise Time			65	104	ns
$t_{d(off)}$	Turn-Off Delay Time			75	120	ns
t_f	Fall Time			30	48	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 40 V, I_D = 36 A		195	273	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 8 V; V_{DD} = 40 V, I_D = 36 A		159	223	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 40 V, I_D = 36 A		69		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 40 V, I_D = 36 A		36		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.6 A (Note 2)		0.7	1.1	V
		V_{GS} = 0 V, I_S = 36 A (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	I_F = 36 A, di/dt = 100 A/μs		81	130	ns
Q_{rr}	Reverse Recovery Charge			88	141	nC

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Top Source)	1.6	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Bottom Drain)	0.8	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	26	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1e)	14	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1f)	16	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1h)	60	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1k)	9	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1l)	11	

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta CA}$ is determined by the user's board design.



a. 38 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 81 °C/W when mounted on a minimum pad of 2 oz copper

c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper

d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper

e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in^2 pad of 2 oz copper

f. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

g. 200FPM Airflow, No Heat Sink,1 in^2 pad of 2 oz copper

h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper

i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper

j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper

k. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in^2 pad of 2 oz copper

l. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. E_{AS} of 1734 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 34 A, V_{DD} = 80 V, V_{GS} =10 V. 100% test at L = 0.3 mH, I_{AS} = 75 A.

4. Pulsed Id please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25 °C unless otherwise noted.

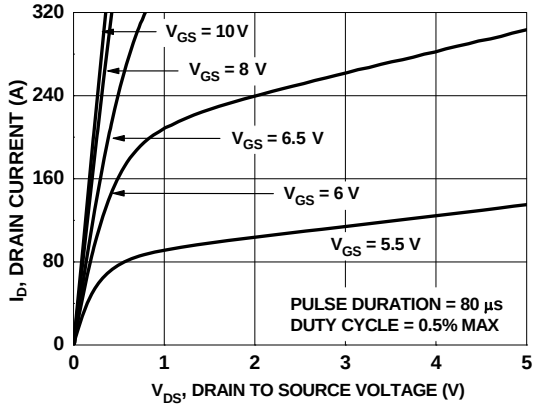


Figure 1. On-Region Characteristics

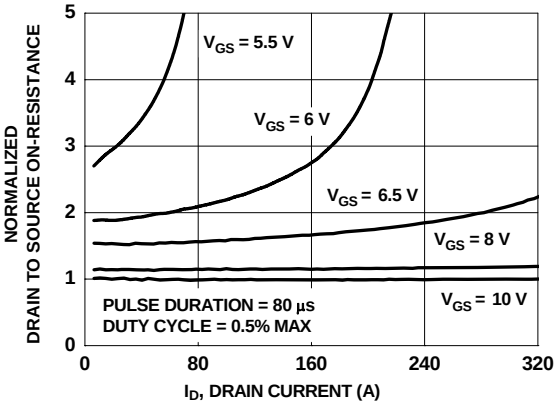


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

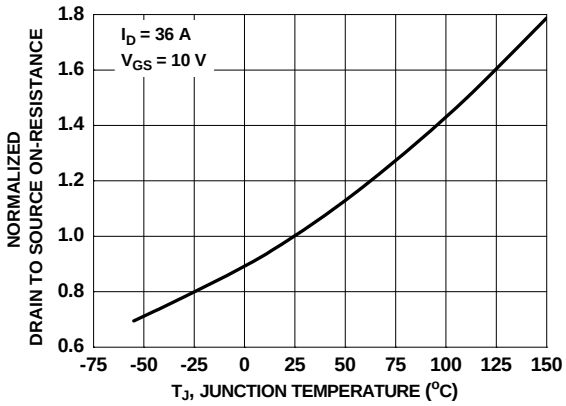


Figure 3. Normalized On-Resistance vs. Junction Temperature

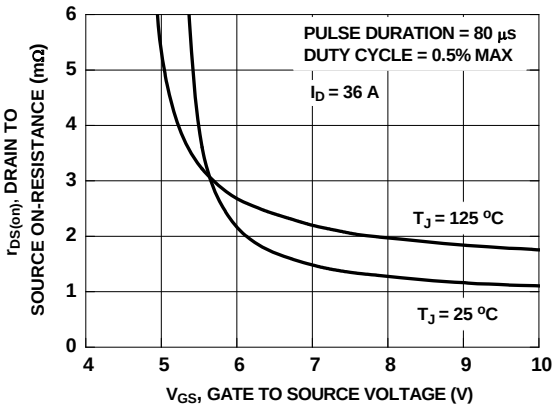


Figure 4. On-Resistance vs. Gate to Source Voltage

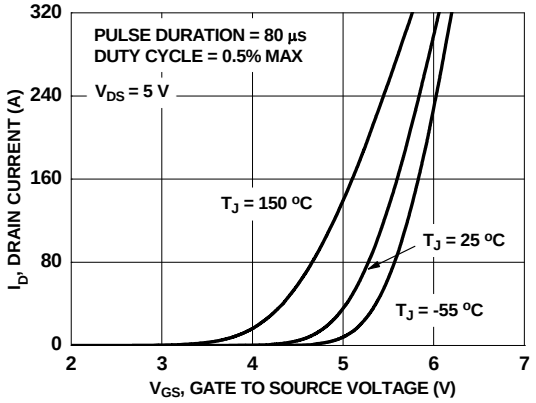


Figure 5. Transfer Characteristics

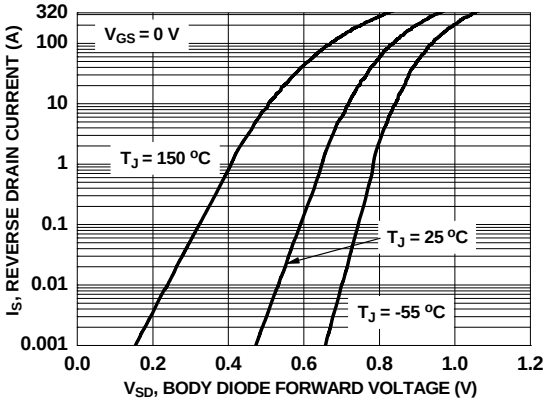


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted.

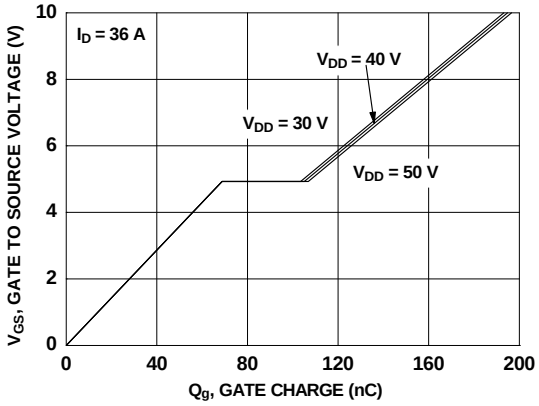


Figure 7. Gate Charge Characteristics

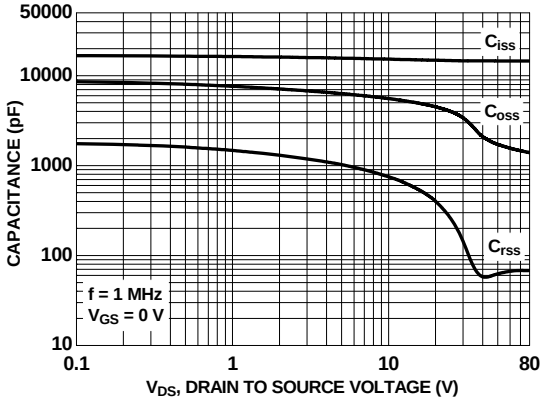


Figure 8. Capacitance vs. Drain to Source Voltage

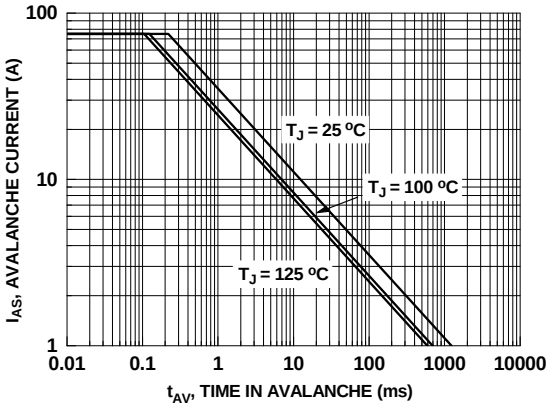


Figure 9. Unclamped Inductive Switching Capability

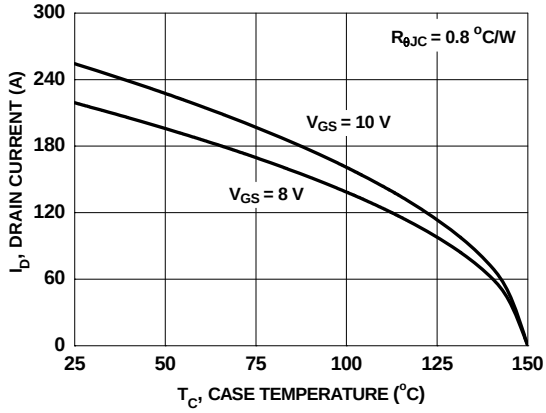


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

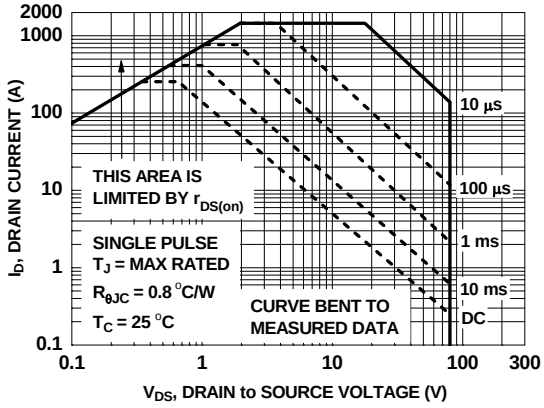


Figure 11. Forward Bias Safe Operating Area

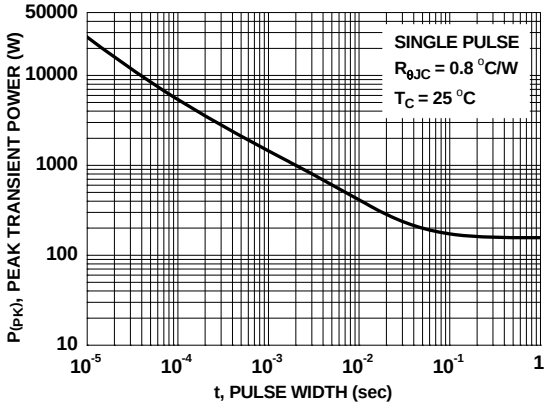


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted.

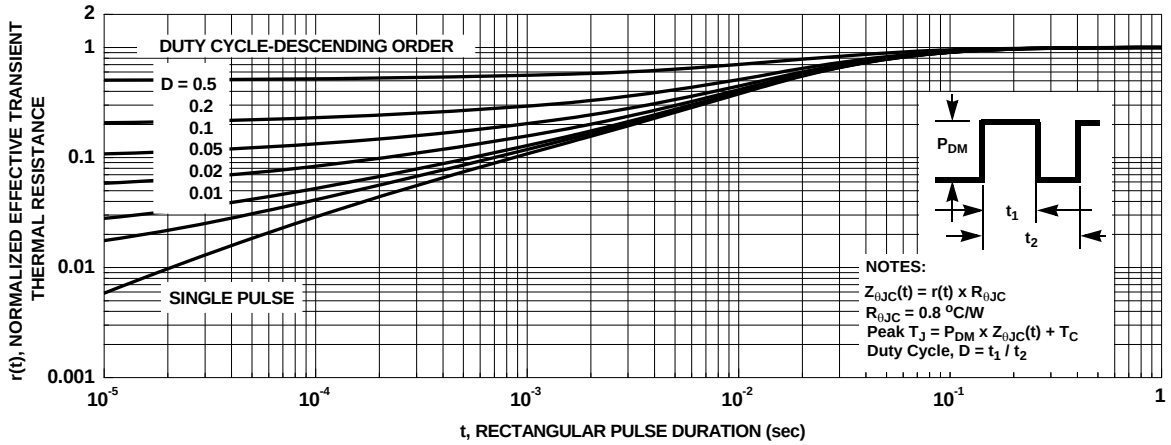
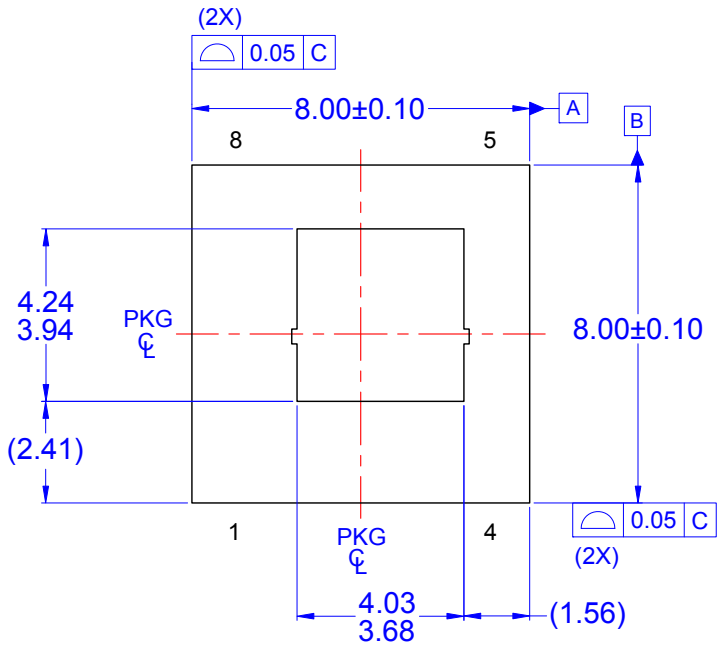
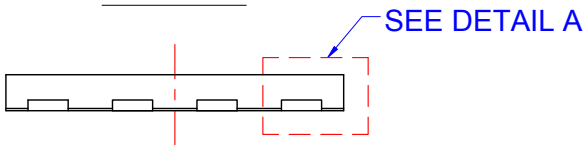


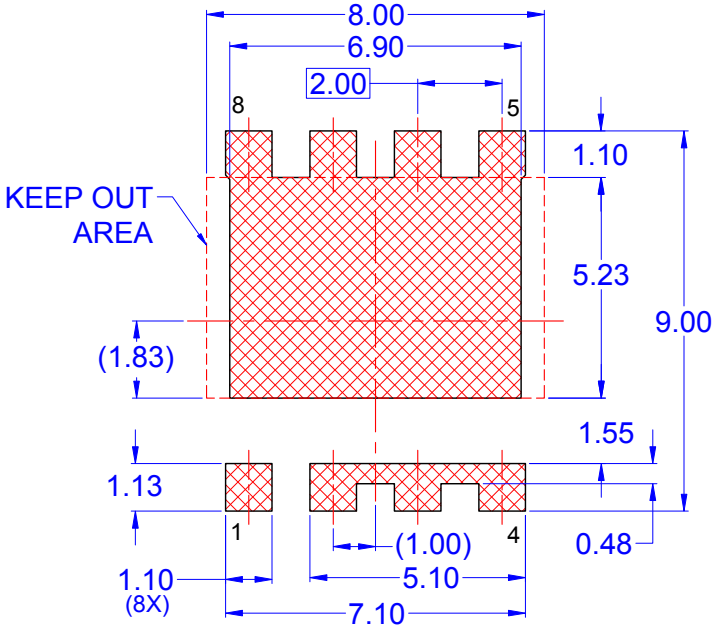
Figure 13. Junction-to-Case Transient Thermal Response Curve



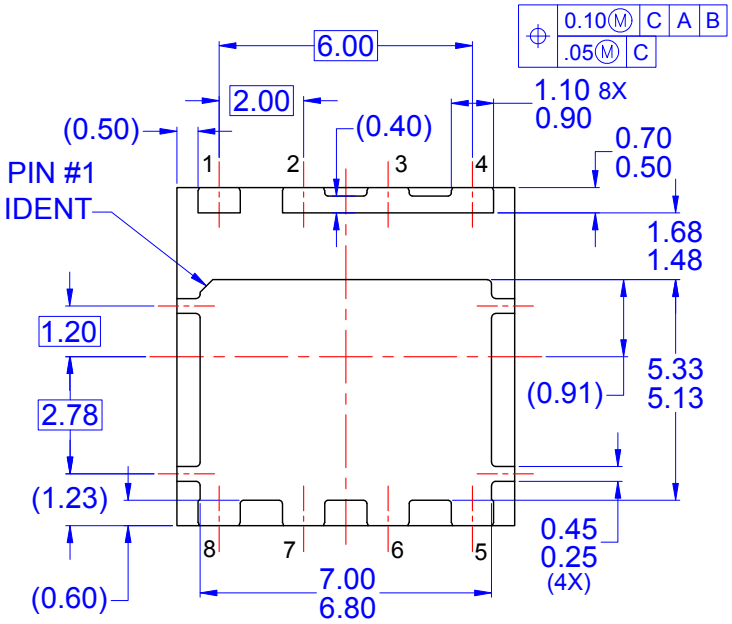
TOP VIEW



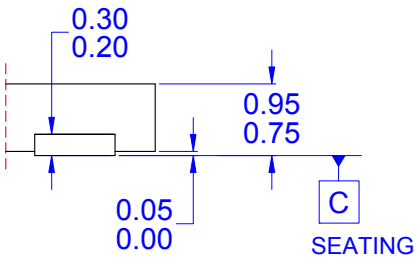
FRONT VIEW



LAND PATTERN
RECOMMENDATION



BOTTOM VIEW



DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE IS NOT PRESENTLY REGISTERED WITH ANY STANDARDS COMMITTEE.

B) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR PROTRUSIONS.

C) ALL DIMENSIONS ARE IN MILLIMETERS.

D) DRAWING CONFORMS TO ASME Y14.5M-2009.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUR AREA.

F) DRAWING FILENAME: MKT-PQFN08RREV2

FAIRCHILD™

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative