


### General Description

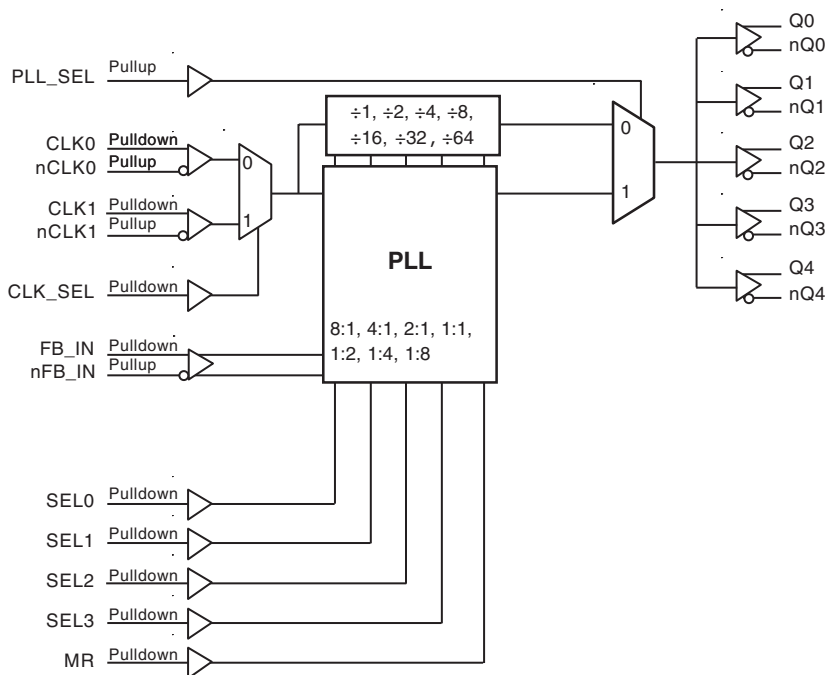


The ICS8745BI is a highly versatile 1:5 LVDS Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8745BI has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 31.25MHz to 700MHz. The Reference Divider, Feedback Divider and Output Divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL\_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

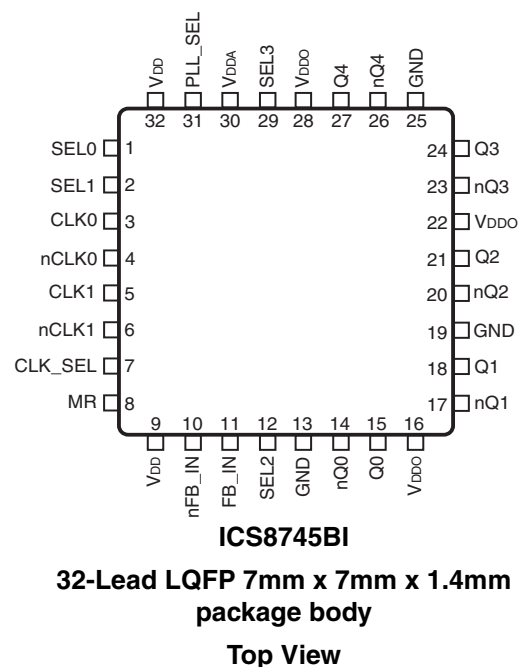
### Features

- Five differential LVDS outputs designed to meet or exceed the requirements of ANSI TIA/EIA-644
- Selectable differential clock inputs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Output frequency range: 31.25MHz to 700MHz
- Input frequency range: 31.25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Cycle-to-cycle jitter: 30ps (maximum)
- Output skew: 40ps (maximum)
- Static phase offset: 25ps ± 125ps
- Full 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

### Block Diagram



### Pin Assignment



**Table 1. Pin Descriptions**

| Number       | Name                     | Type   |          | Description  |
|--------------|--------------------------|--------|----------|--|
| 1, 2, 12, 29 | SEL0, SEL1, SEL2 SEL3    | Input  | Pulldown | Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels.   |
| 3            | CLK0                     | Input  | Pulldown | Non-inverting differential clock input.  |
| 4            | nCLK0                    | Input  | Pullup   | Inverting differential clock input.  |
| 5            | CLK1                     | Input  | Pulldown | Non-inverting differential clock input.  |
| 6            | nCLK1                    | Input  | Pullup   | Inverting differential clock input.  |
| 7            | CLK_SEL                  | Input  | Pulldown | Clock select input. When HIGH, selects CLK1,nCLK1. When LOW, selects CLK0, nCLK0. LVCMOS / LVTTTL interface levels.  |
| 8            | MR                       | Input  | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels. |
| 9, 32        | V <sub>DD</sub>          | Power  |          | Core supply pins.  |
| 10           | $\overline{\text{FBIN}}$ | Input  | Pullup   | Inverting differential feedback input to phase detector for regenerating clocks with "Zero Delay."   |
| 11           | FBIN                     | Input  | Pulldown | Non-inverted differential feedback input to phase detector for regenerating clocks with "Zero Delay."  |
| 13, 19, 25   | GND                      | Power  |          | Power supply ground.   |
| 14, 15       | nQ0/Q0                   | Output |          | Differential output pair. LVDS interface levels.   |
| 16, 22, 28   | V <sub>DDO</sub>         | Power  |          | Output supply pins.  |
| 17, 18       | nQ1/Q1                   | Output |          | Differential output pair. LVDS interface levels.   |
| 20, 21       | nQ2/Q2                   | Output |          | Differential output pair. LVDS interface levels.   |
| 23, 24       | nQ3/Q3                   | Output |          | Differential output pair. LVDS interface levels.   |
| 26, 27       | nQ4/Q4                   | Output |          | Differential output pair. LVDS interface levels.   |
| 30           | V <sub>DDA</sub>         | Power  |          | Analog supply pin.   |
| 31           | PLL_SEL                  | Input  | Pullup   | PLL select. Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. LVCMOS/LVTTTL interface levels.   |

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 4       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | kΩ    |

## Function Tables

**Table 3A. Control Input Function Table**

| Inputs |      |      |      |                                  | Outputs<br>PLL_SEL = 1<br>PLL Enable Mode |
|--------|------|------|------|----------------------------------|---|
| SEL3   | SEL2 | SEL1 | SEL0 | Reference Frequency Range (MHz)* | Q[0:4], nQ[0:4]                           |
| 0z     | 0    | 0    | 0    | 250 - 700                        | ÷1  |
| 0      | 0    | 0    | 1    | 125 - 350                        | ÷1  |
| 0      | 0    | 1    | 0    | 62.5 - 175                       | ÷1  |
| 0      | 0    | 1    | 1    | 31.25 - 87.5                     | ÷1  |
| 0      | 1    | 0    | 0    | 250 - 700                        | ÷2  |
| 0      | 1    | 0    | 1    | 125 - 350                        | ÷2  |
| 0      | 1    | 1    | 0    | 62.5 - 175                       | ÷2  |
| 0      | 1    | 1    | 1    | 250 - 700                        | ÷4  |
| 1      | 0    | 0    | 0    | 125 - 350                        | ÷4  |
| 1      | 0    | 0    | 1    | 250 - 700                        | ÷8  |
| 1      | 0    | 1    | 0    | 125 - 350                        | x2  |
| 1      | 0    | 1    | 1    | 62.5 - 175                       | x2  |
| 1      | 1    | 0    | 0    | 31.25 - 87.5                     | x2  |
| 1      | 1    | 0    | 1    | 62.5 - 175                       | x4  |
| 1      | 1    | 1    | 0    | 31.25 - 87.5                     | x4  |
| 1      | 1    | 1    | 1    | 31.25 - 87.5                     | x8  |

\*NOTE: VCO frequency range for all configurations above is 250MHz to 700MHz.

**Table 3B. PLL Bypass Function Table**

| Inputs |      |      |      | Outputs<br>PLL_SEL = 0<br>PLL Bypass Mode |
|--------|------|------|------|---|
| SEL3   | SEL2 | SEL1 | SEL0 | Q[0:4], nQ[0:4]                           |
| 0z     | 0    | 0    | 0    | ÷4  |
| 0      | 0    | 0    | 1    | ÷4  |
| 0      | 0    | 1    | 0    | ÷4  |
| 0      | 0    | 1    | 1    | ÷8  |
| 0      | 1    | 0    | 0    | ÷8  |
| 0      | 1    | 0    | 1    | ÷8  |
| 0      | 1    | 1    | 0    | ÷16                                       |
| 0      | 1    | 1    | 1    | ÷16                                       |
| 1      | 0    | 0    | 0    | ÷32                                       |
| 1      | 0    | 0    | 1    | ÷64                                       |
| 1      | 0    | 1    | 0    | ÷2  |
| 1      | 0    | 1    | 1    | ÷2  |
| 1      | 1    | 0    | 0    | ÷4  |
| 1      | 1    | 0    | 1    | ÷1  |
| 1      | 1    | 1    | 0    | ÷2  |
| 1      | 1    | 1    | 1    | ÷1  |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item  | Rating                   |
|---|--------------------------|
| Supply Voltage, $V_{DD}$                              | 4.6V                     |
| Inputs, $V_I$   | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, $I_O$<br>Continuous Current<br>Surge Current | 10mA<br>15mA             |
| Package Thermal Impedance, $\theta_{JA}$              | 47.9°C/W (0 lfpm)        |
| Storage Temperature, $T_{STG}$                        | -65°C to 150°C           |

## DC Electrical Characteristics

**Table 4A. LVDS Power Supply DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol    | Parameter             | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDA}$ | Analog Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{DD}$  | Power Supply Current  |                 |         |         | 128     | mA    |
| $I_{DDA}$ | Analog Supply Current |                 |         |         | 18      | mA    |
| $I_{DDO}$ | Output Supply Current |                 |         |         | 62      | mA    |

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$**

| Symbol   | Parameter          | Test Conditions          | Minimum                        | Typical | Maximum        | Units   |
|----------|--------------------|--------------------------|--------------------------------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage |                          | 2                              |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  |                          | -0.3                           |         | 0.8            | V       |
| $I_{IH}$ | Input High Current | CLK_SEL,<br>SEL[0:3], MR | $V_{DD} = V_{IN} = 3.465V$     |         | 150            | $\mu A$ |
|          |                    | PLL_SEL                  | $V_{DD} = V_{IN} = 3.465V$     |         | 5              | $\mu A$ |
| $I_{IL}$ | Input Low Current  | CLK_SEL,<br>SEL[0:3], MR | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5      |                | $\mu A$ |
|          |                    | PLL_SEL                  | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150    |                | $\mu A$ |

**Table 4C. Differential DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol    | Parameter                            |                      | Test Conditions                      | Minimum   | Typical | Maximum         | Units         |
|-----------|--------------------------------------|----------------------|--------------------------------------|-----------|---------|-----------------|---------------|
| $I_{IH}$  | Input High Current                   | CLK0, CLK1, FB_IN    | $V_{DD} = V_{IN} = 3.465V$           |           |         | 150             | $\mu\text{A}$ |
|           |                                      | nCLK0, nCLK1, nFB_IN | $V_{DD} = V_{IN} = 3.465V$           |           |         | 5               | $\mu\text{A}$ |
| $I_{IL}$  | Input Low Current                    | CLK0, CLK1, FB_IN    | $V_{DD} = 3.465V$ ,<br>$V_{IN} = 0V$ | -5        |         |                 | $\mu\text{A}$ |
|           |                                      | nCLK0, nCLK1, nFB_IN | $V_{DD} = 3.465V$ ,<br>$V_{IN} = 0V$ | -150      |         |                 | $\mu\text{A}$ |
| $V_{PP}$  | Peak-to-Peak Voltage; NOTE 1         |                      |                                      | 0.15      |         | 1.3             | V             |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 |                      |                                      | GND + 0.5 |         | $V_{DD} - 0.85$ | V             |

NOTE 1:  $V_{IL}$  should not be less than -0.3VNOTE 2: For single-ended applications, the maximum input voltage for CLKx, nCLKx is  $V_{DD} + 0.3V$ .**Table 4D. LVDS DC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol          | Parameter                   | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| $V_{OD}$        | Differential Output Voltage |                 | 320     | 440     | 550     | mV    |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change   |                 |         | 0       | 50      | mV    |
| $V_{OS}$        | Offset Voltage              |                 | 1.05    | 1.2     | 1.35    | V     |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change   |                 |         |         | 25      | mV    |

**Table 5. Input Frequency Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

| Symbol   | Parameter       |                        | Test Conditions | Minimum | Typical | Maximum | Units         |
|----------|-----------------|------------------------|-----------------|---------|---------|---------|---------------|
| $F_{IN}$ | Input Frequency | CLK0/nCLK0, CLK1/nCLK1 | PLL_SEL = 1     | 31.25   |         | 700     | $\mu\text{A}$ |
|          |                 |                        | PLL_SEL = 0     |         |         | 700     | V             |

## AC Electrical Characteristics

**Table 6. AC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

| Symbol                         | Parameter                        | Test Conditions                      | Minimum | Typical | Maximum  | Units |
|--------------------------------|----------------------------------|--------------------------------------|---------|---------|----------|-------|
| $f_{MAX}$                      | Output Frequency                 |                                      |         |         | 700      | MHz   |
| $t_{PD}$                       | Propagation Delay; NOTE 1        | PLL_SEL = 0V, $f \leq 700\text{MHz}$ | 2.9     | 3.4     | 4.0      | ns    |
| $t_{sk}(\emptyset)$            | Static Phase Offset; NOTE 2, 5   | PLL_SEL = 3.3V                       | -100    | 25      | 150      | ps    |
| $t_{sk}(o)$                    | Output Skew; NOTE 3, 5           |                                      |         |         | 40       | ps    |
| $\overset{\sim}{f}jit(cc)$     | Cycle-to-Cycle Jitter; NOTE 5, 6 |                                      |         |         | 30       | ps    |
| $\overset{\sim}{f}jit(\theta)$ | Phase Jitter; NOTE 4, 5, 6       |                                      |         |         | $\pm 52$ | ps    |
| $t_L$                          | PLL Lock Time                    |                                      |         |         | 1        | ms    |
| $t_R / t_F$                    | Output Rise/Fall Time; NOTE 7    | 20% to 80%                           | 200     |         | 700      | ps    |
| odc                            | Output Duty Cycle                |                                      | 45      | 50      | 55       | %     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions..

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal across all conditions, when the PLL is locked and the input reference frequency is stable.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

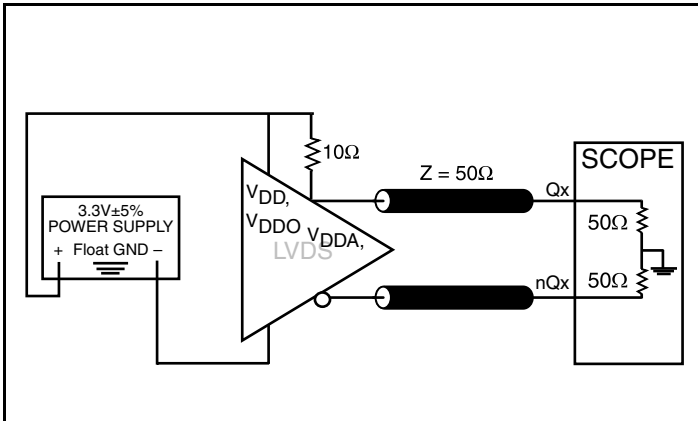
NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

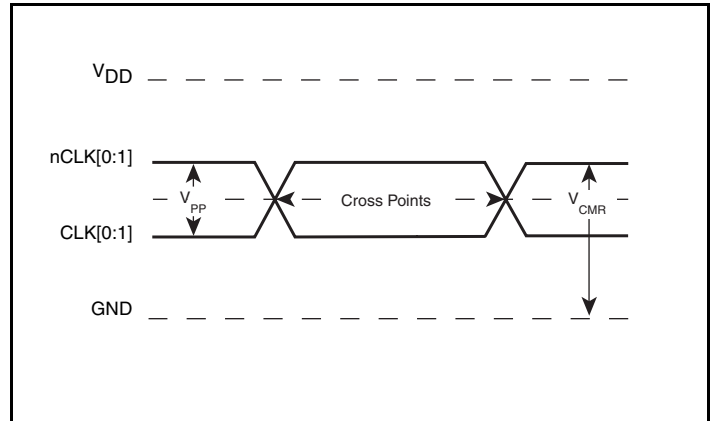
NOTE 6: Characterized at VCO frequency of 622MHz.

NOTE 7: Measured from the 20% to 80% points. Guaranteed by characterization. Not production tested.

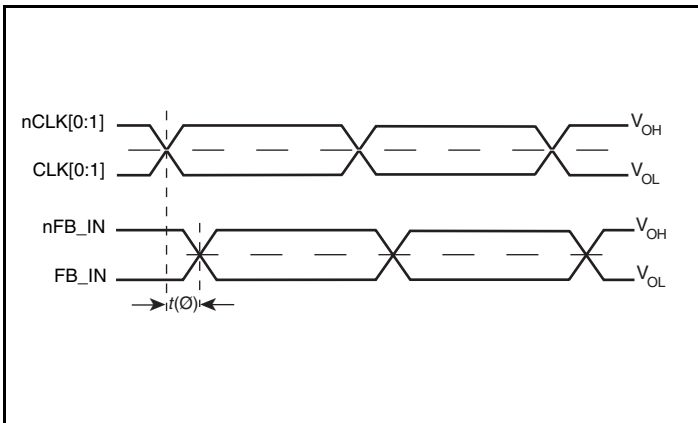
### Parameter Measurement Information



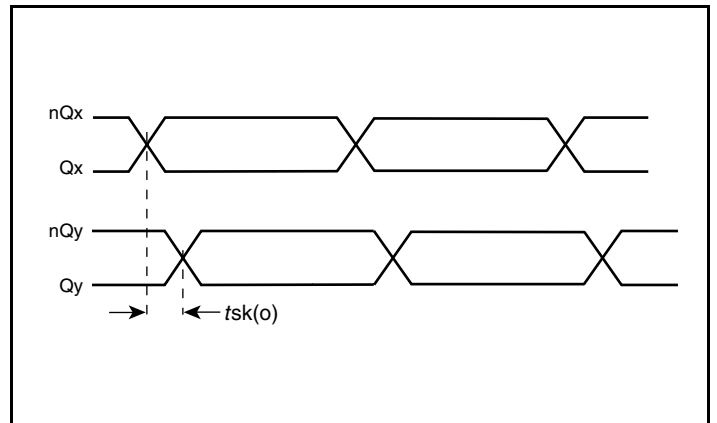
3.3V LVDS Output Load AC Test Circuit



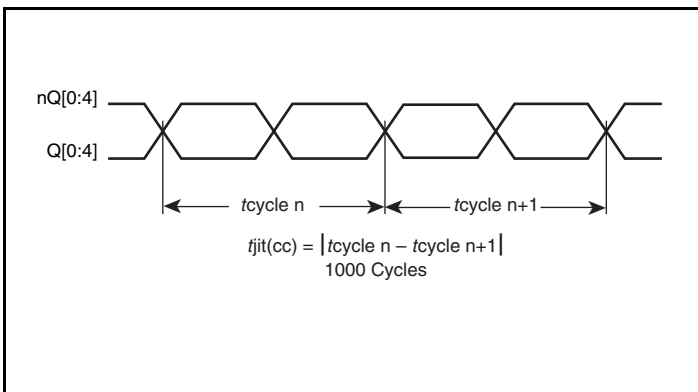
Differential Input Level



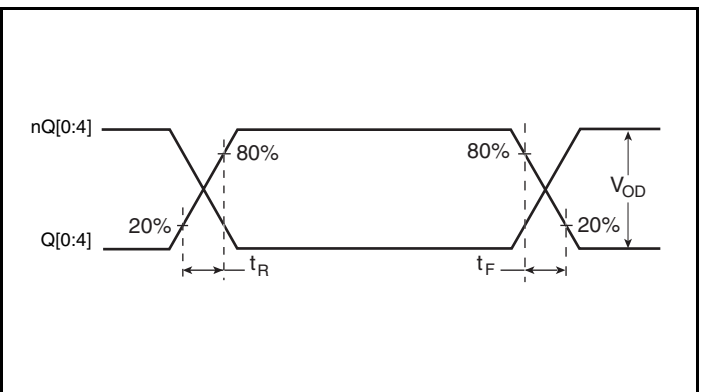
Phase Jitter and Static Phase Offset



Output Skew



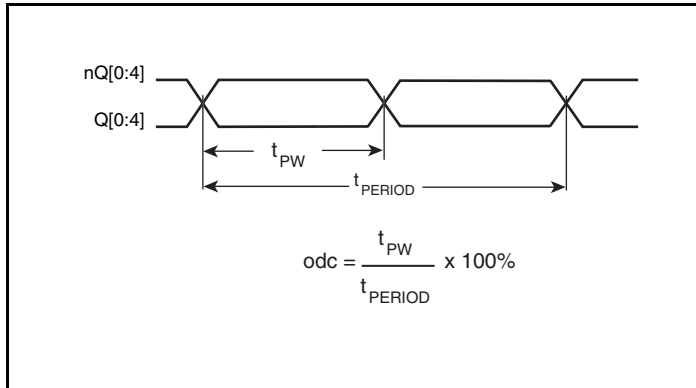
Cycle-to-Cycle Jitter



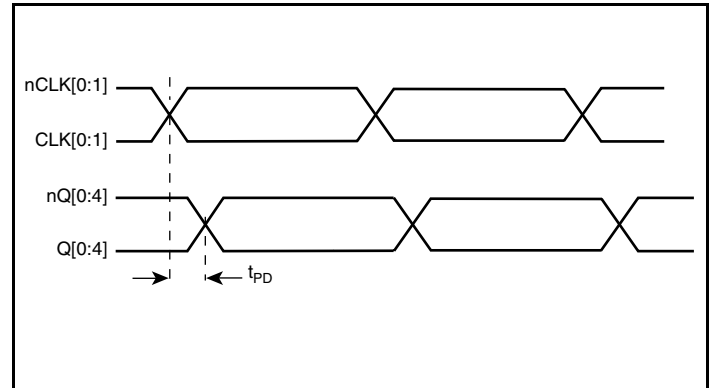
Output Rise/Fall Time



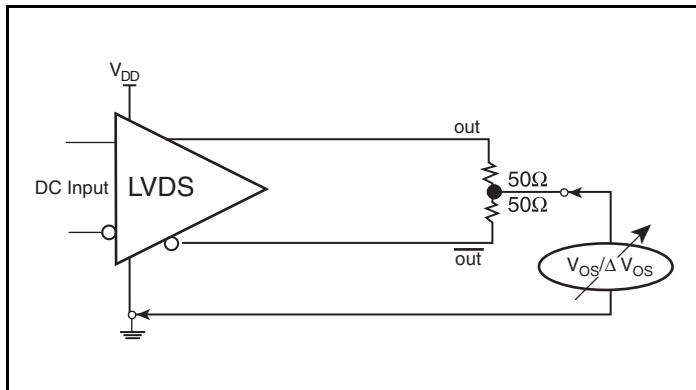
## Parameter Measurement Information, continued



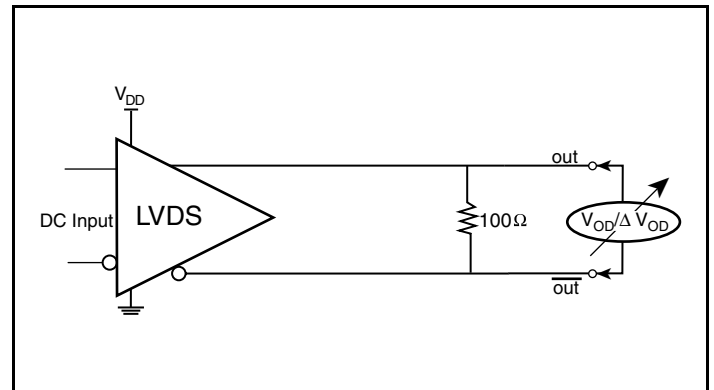
**Output Duty Cycle**



**Propagation Delay**



**Offset Voltage Setup**

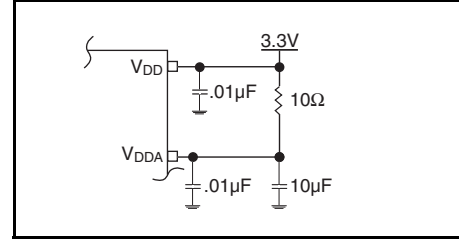


**Differential Output Voltage Setup**

## Application Information

### Power Supply Filtering Technique

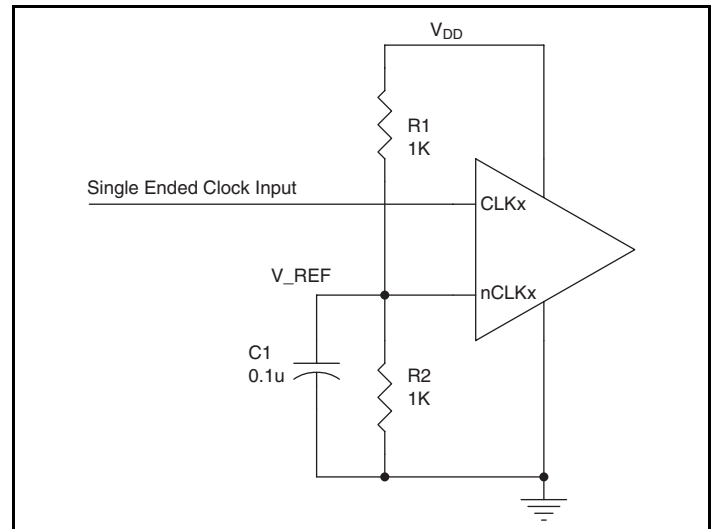
As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8745BI provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$  and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{DDA}$  pin.



**Figure 1. Power Supply Filtering**

### Wiring the Differential Input to Accept Single Ended Levels

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors  $R1$ ,  $R2$  and  $C1$ . This bias circuit should be located as close as possible to the input pin. The ratio of  $R1$  and  $R2$  might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only  $2.5\text{V}$  and  $V_{DD} = 3.3\text{V}$ ,  $V_{REF}$  should be  $1.25\text{V}$  and  $R2/R1 = 0.609$ .

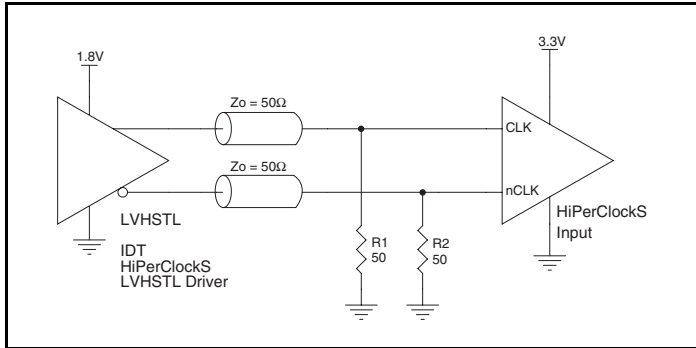


**Figure 2. Single-Ended Signal Driving Differential Input**

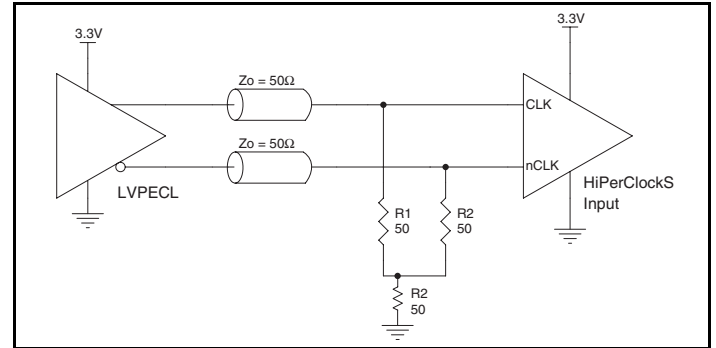
### Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3F show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

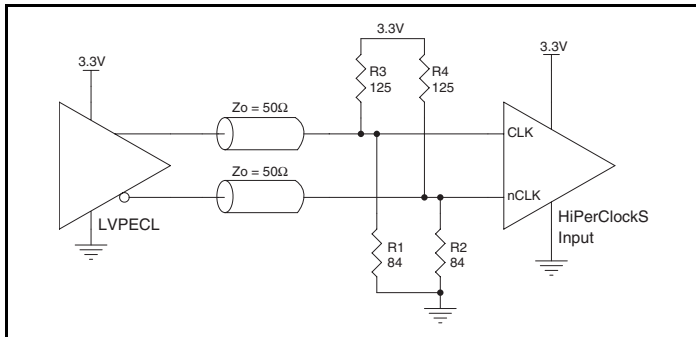
Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



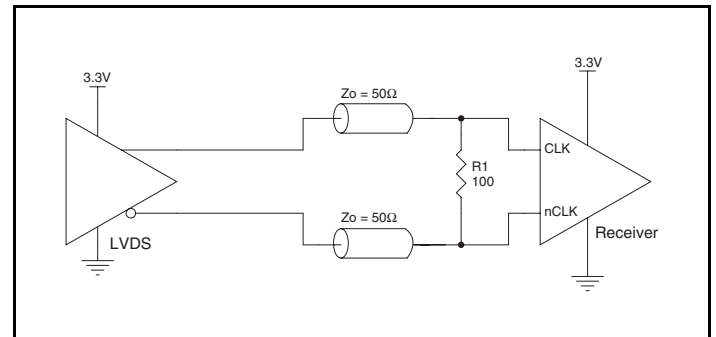
**3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver**



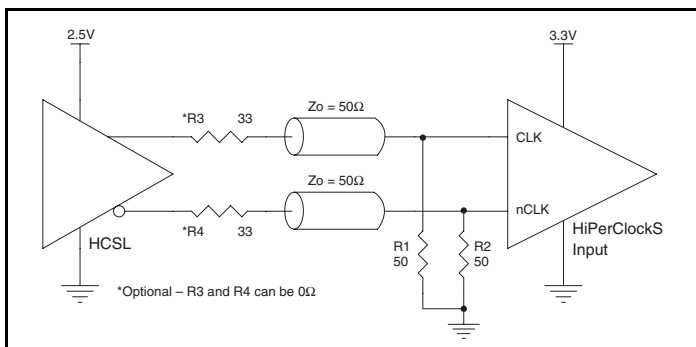
**Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



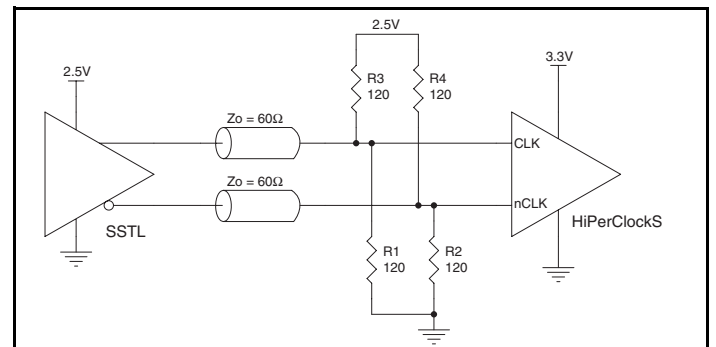
**Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver**



**Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver**



**Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### CLK/nCLK Input

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from CLK to ground.

### Outputs:

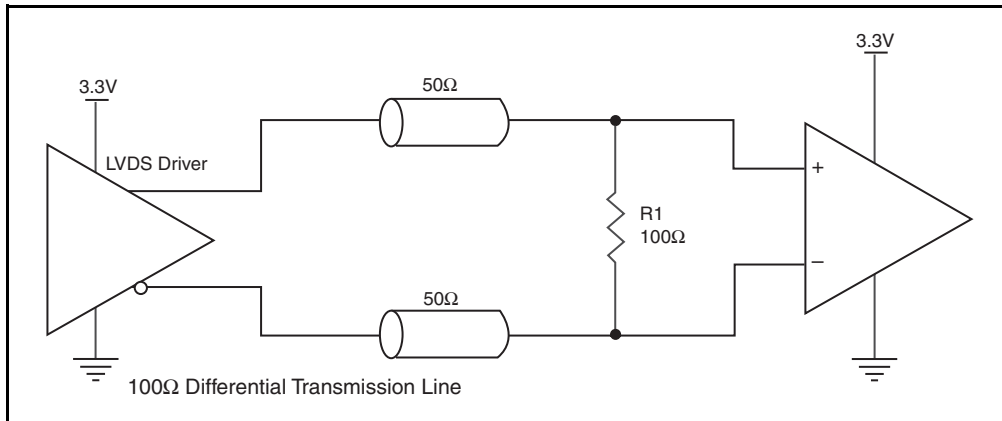
#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100 $\Omega$  across. If they are left floating, we recommend that there is no trace attached.

## 3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4*. In a 100 $\Omega$  differential transmission line environment, LVDS drivers require a matched load termination of 100 $\Omega$  across near the receiver input. For a multiple

LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.



**Figure 4. Typical LVDS Driver Termination**

### Schematic Example

The schematic of the ICS8745BI layout example is shown in *Figure 5A*. The ICS8745BI recommended PCB board layout for this example is shown in *Figure 5B*. This layout example is used as a general

guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

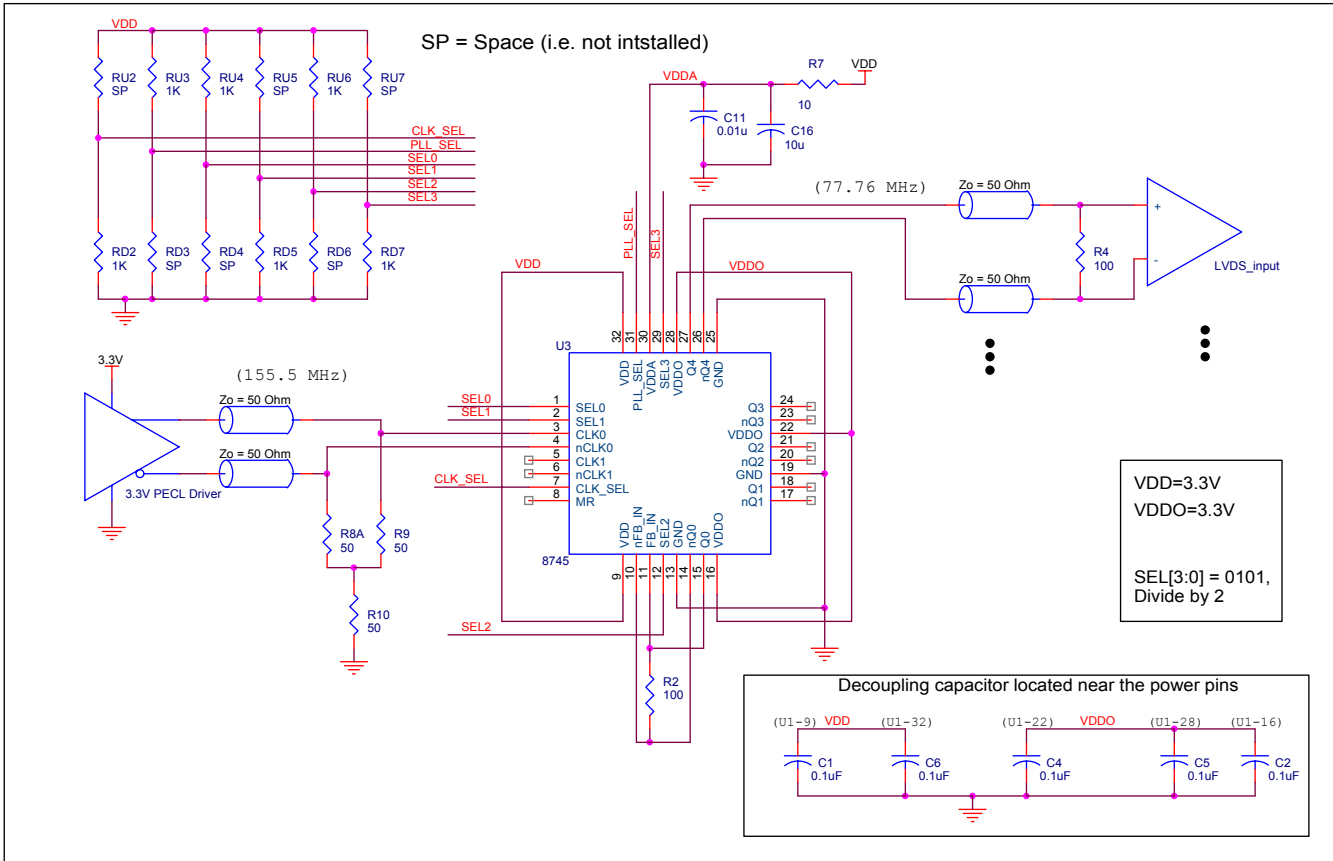


Figure 5A. ICS8745BI LVDS Zero Delay Buffer Schematic Example

The following component footprints are used in this layout example.

All the resistors and capacitors are size 0603.

### Power and Grounding

Place the decoupling capacitors as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the  $V_{DDA}$  pin as possible.

### Clock Traces and Termination

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be

restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have the same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

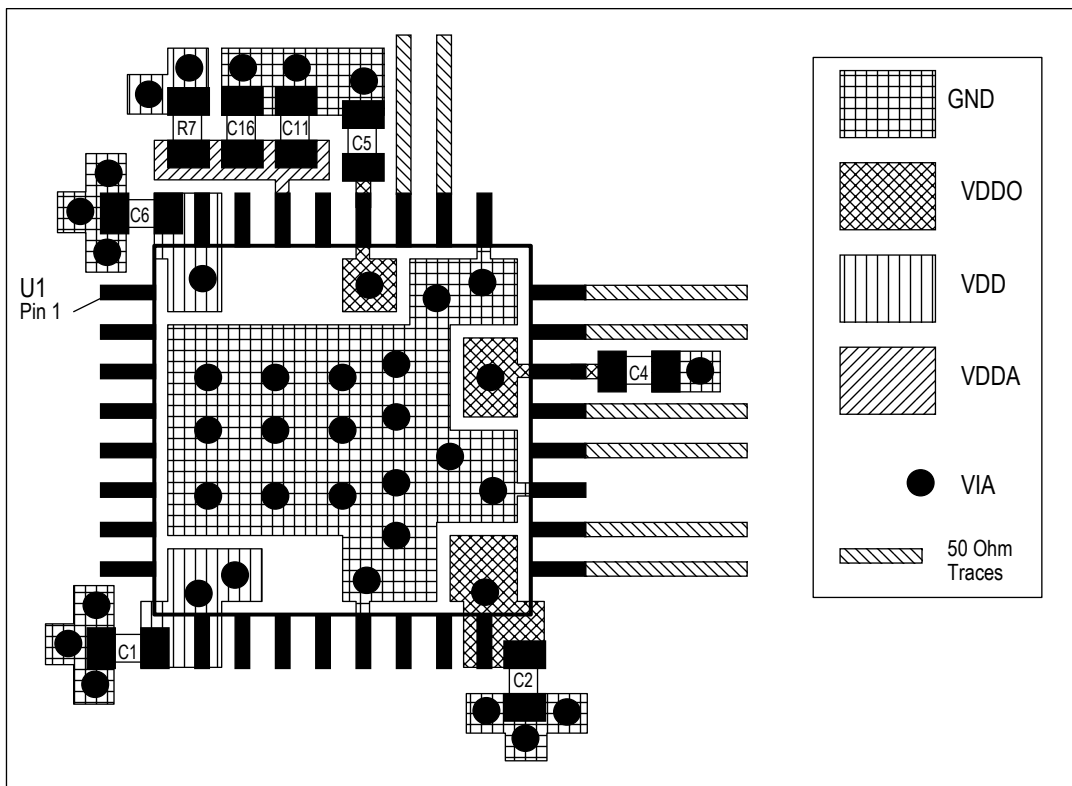


Figure 5B. PCB Board Layout for ICS8745BI

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8745BI. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8745BI is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (128mA + 18mA) = \mathbf{506mW}$
- Power (outputs)<sub>MAX</sub> =  $V_{DDO\_MAX} * I_{DDO\_MAX} = 3.465V * 62mA = \mathbf{215mW}$

**Total Power<sub>MAX</sub> = 506mW + 215mW = 721mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.721\text{W} * 42.1^\circ\text{C/W} = 115.3^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance  $\theta_{JA}$  for 32 Lead LQFP, Forced Convection**

| $\theta_{JA}$ vs. Air Flow                   |          |          |          |
|--|----------|----------|----------|
| Linear Feet per Minute                       | 0        | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards  | 47.9°C/W | 42.1°C/W | 39.4°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

## Reliability Information

**Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 32 Lead LQFP**

| $\theta_{JA}$ vs. Air Flow   |          |          |          |
|--|----------|----------|----------|
| Linear Feet per Minute   | 0        | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards   | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards  | 47.9°C/W | 42.1°C/W | 39.4°C/W |
| NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. |          |          |          |

## Transistor Count

The transistor count for ICS8745BI is: 2772



## Package Outline and Package Dimensions

### Package Outline - Y Suffix for 32 Lead LQFP

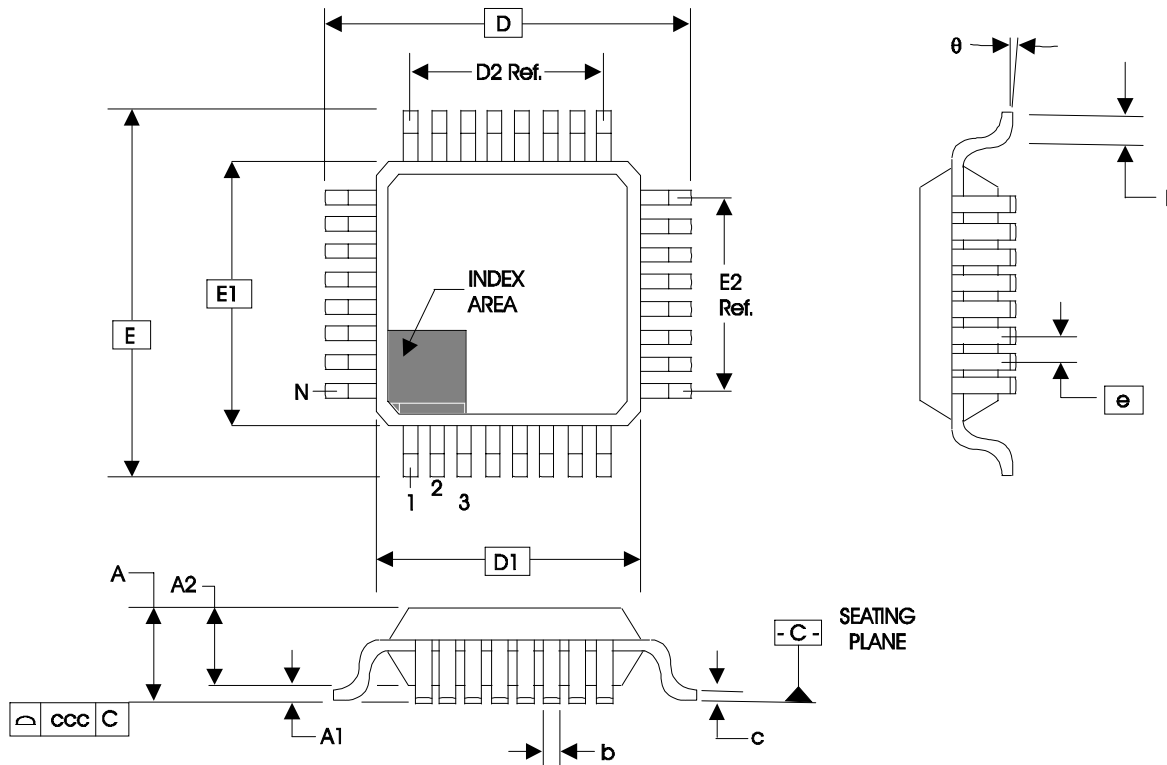


Table 9. Package Dimensions for 32 Lead LQFP

| JEDEC Variation: BBC - HD     |            |         |         |
|-------------------------------|------------|---------|---------|
| All Dimensions in Millimeters |            |         |         |
| Symbol                        | Minimum    | Nominal | Maximum |
| <b>N</b>                      | 32         |         |         |
| <b>A</b>                      |            |         | 1.60    |
| <b>A1</b>                     | 0.05       | 0.10    | 0.15    |
| <b>A2</b>                     | 1.35       | 1.40    | 1.45    |
| <b>b</b>                      | 0.30       | 0.37    | 0.45    |
| <b>c</b>                      | 0.09       |         | 0.20    |
| <b>D &amp; E</b>              | 9.00 Basic |         |         |
| <b>D1 &amp; E1</b>            | 7.00 Basic |         |         |
| <b>D2 &amp; E2</b>            | 5.60 Ref.  |         |         |
| <b>e</b>                      | 0.80 Basic |         |         |
| <b>L</b>                      | 0.45       | 0.60    | 0.75    |
| <b>θ</b>                      | 0°         |         | 7°      |
| <b>ccc</b>                    |            |         | 0.10    |

Reference Document: JEDEC Publication 95, MS-026

## Ordering Information

**Table 10. Ordering Information**

| Part/Order Number | Marking      | Package                  | Shipping Packaging | Temperature   |
|-------------------|--------------|--------------------------|--------------------|---------------|
| 8745BYI           | ICS8745BYI   | 32 Lead LQFP             | Tray               | -40°C to 85°C |
| 8745BYIT          | ICS8745BYI   | 32 Lead LQFP             | 1000 Tape & Reel   | -40°C to 85°C |
| 8745BYILF         | ICS8745BYILF | "Lead-Free" 32 Lead LQFP | Tray               | -40°C to 85°C |
| 8745BYILFT        | ICS8745BYILF | "Lead-Free" 32 Lead LQFP | 1000 Tape & Reel   | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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## Revision History Sheet

| Rev | Table            | Page                    | Description of Change  | Date    |
|-----|------------------|-------------------------|--|---------|
| B   | T4D              | 5                       | LVDS DC Characteristics Table - modified VOS 0.90V min. to 1.05V min, 1.15V typical to 1.2V typical, and 1.4V max. to 1.35V max.   | 3/17/04 |
| C   | T6               | 7<br>15                 | AC Characteristics Table - changed $t_{PD}$ max limit from 3.9ns to 4.0ns.<br>Added Power Considerations section.<br>Updated format throughout the datasheet.  | 4/16/07 |
| D   | T4C<br>T6<br>T10 | 1<br>6<br>7<br>11<br>18 | Pin Assignment - corrected pin 14 from Q0 to nQ0. Missed error when converted to new format on April 16, 2007 from March 17, 2004.<br>Differential DC Characteristics Table - replaced NOTE 1 with new note.<br>AC Characteristics Table - added thermal note.<br>Updated <i>Differential Clock Input Interface section</i> .<br>Ordering Information Table - Part/Order Number - deleted "ICS" prefix.<br>Updated Header/Footer throughout the document and contact page. | 6/4/09  |



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