# P89LPC9402

## 8-bit microcontroller with accelerated two-clock 80C51 core 8 kB 3 V byte-erasable flash with 32 segment 4 LCD driver

**Rev. 01 — 22 April 2009**                    **Product data sheet**

## 1. General description

The P89LPC9402 is a multi-chip module consisting of a P89LPC931A1 single-chip microcontroller combined with a PCF8576D universal LCD driver in a low-cost 64-pin package. The LCD driver provides 32 segments and supports from 1 to 4 backplanes. Display overhead is minimized by an on-chip display RAM with auto-increment addressing.

## 2. Features

### 2.1 Principal features

- 8 kB byte-erasable flash code memory organized into 1 kB sectors and 64-byte pages. Single-byte erasing allows any byte(s) to be used as non-volatile data storage.
- 256-byte RAM data memory.
- 32 segment $\times$ 4 backplane LCD controller supports from 1 to 4 backplanes.
- Two analog comparators with selectable inputs and reference source.
- Two 16-bit counter/timers (each may be configured to toggle a port output upon timer overflow or to become a PWM output).
- A 23-bit system timer that can also be used as real-time clock consisting of a 7-bit prescaler and a programmable and readable 16-bit timer.
- Enhanced UART with a fractional baud rate generator, break detect, framing error detection, and automatic address detection; 400 kHz byte-wide I$^2$C-bus communication port and SPI communication port.
- 2.4 V to 3.6 V $V_{DD}$ operating range. I/O pins are 5 V tolerant (may be pulled up or driven to 5.5 V).
- Enhanced low voltage (brownout) detect allows a graceful system shutdown when power fails.
- 64-pin LQFP package with 20 microcontroller I/O pins minimum and up to 23 microcontroller I/O pins while using on-chip oscillator and reset options.

### 2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.

■ Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.

■ Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.

■ In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.

■ Watchdog timer with separate on-chip oscillator, nominal 400 kHz, calibrated to ±5 %, requiring no external components. The watchdog prescaler is selectable from eight values.

■ High-accuracy internal RC oscillator option, with clock doubler option, allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable.

■ Switching on the fly among internal RC oscillator, watchdog oscillator, external clock source provides optimal support of minimal power active mode with fast switching to maximum performance.

■ Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).

■ Active-LOW reset. On-chip power-on reset allows operation without external reset components. A software reset function is also available.

■ Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.

■ Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.

■ Programmable port output configuration options: quasi-bidirectional, open-drain, push-pull, input-only.

■ High current sourcing/sinking (20 mA) on eight I/O pins (P0.3 to P0.7, P1.4, P1.6, P1.7). All other port pins have high sinking capability (20 mA). A maximum limit is specified for the entire chip.

■ Port 'input pattern match' detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.

■ Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.

■ Only power and ground connections are required to operate the P89LPC9402 when internal reset option is selected.

■ Four interrupt priority levels.

■ Eight keypad interrupt inputs, plus two additional external interrupt inputs.

■ Schmitt trigger port inputs.

■ Second data pointer.

■ Emulation support.

■ LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | **Name** | **Description** | | **Version** |
| P89LPC9402FBD | LQFP64 | plastic low profile quad flat package; 64 leads; body 14 × 14 × 1.4 mm | | SOT791-1 |

### 3.1 Ordering options

**Table 2. Part options**

| Type number | Flash memory | Temperature range | Frequency |
|---|---|---|---|
| P89LPC9402FBD | 8 kB | −40 °C to +85 °C | 0 MHz to 18 MHz |

## 4. Block diagram
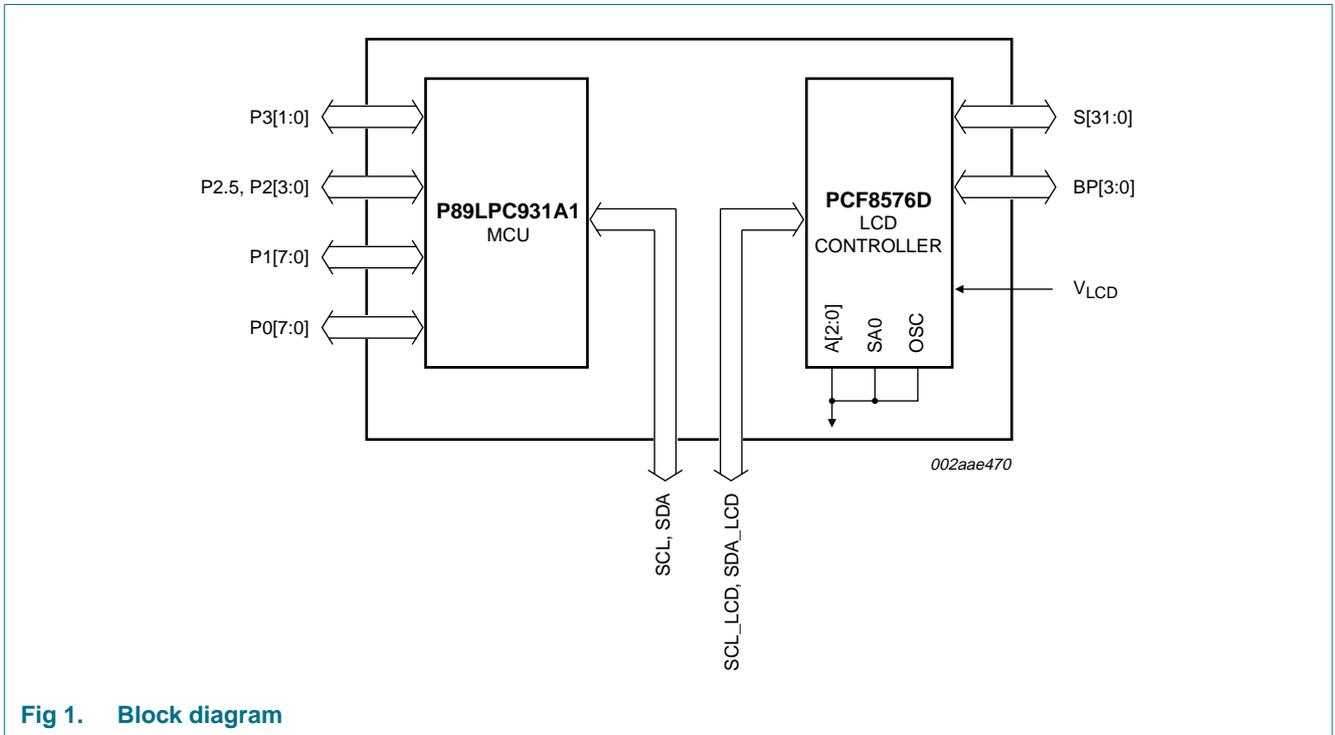


**Fig 1.** Block diagram
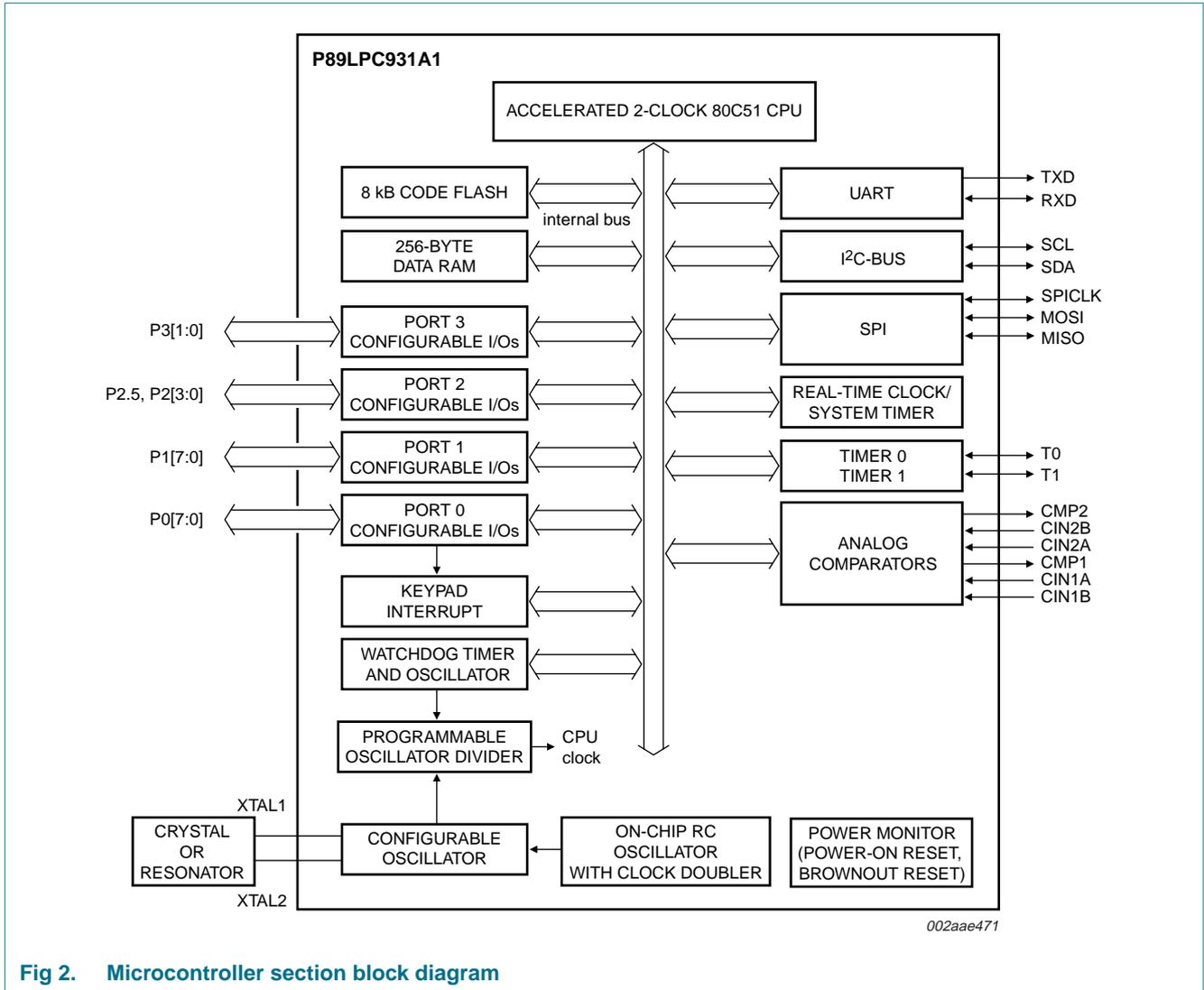
**Fig 2. Microcontroller section block diagram**
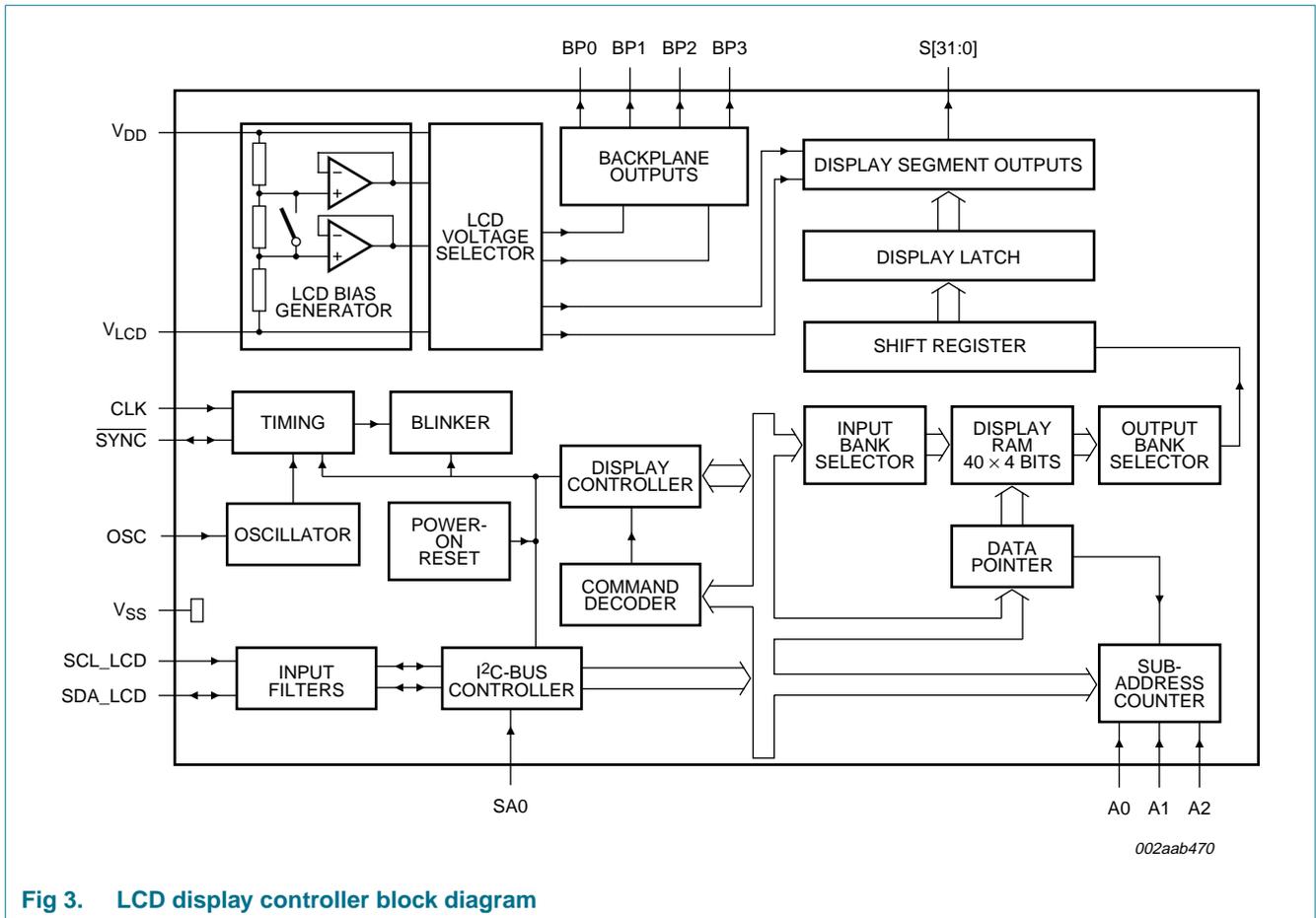
**Fig 3.** LCD display controller block diagram

## 5. Functional diagram
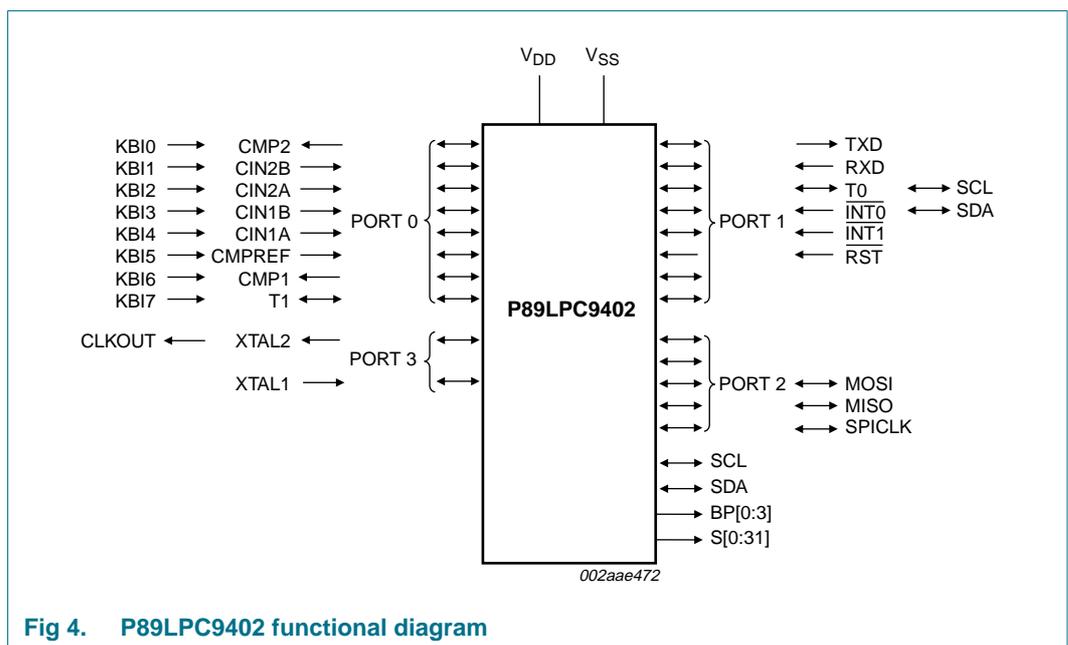


**Fig 4.** P89LPC9402 functional diagram

# 6. Pinning information

## 6.1 Pinning
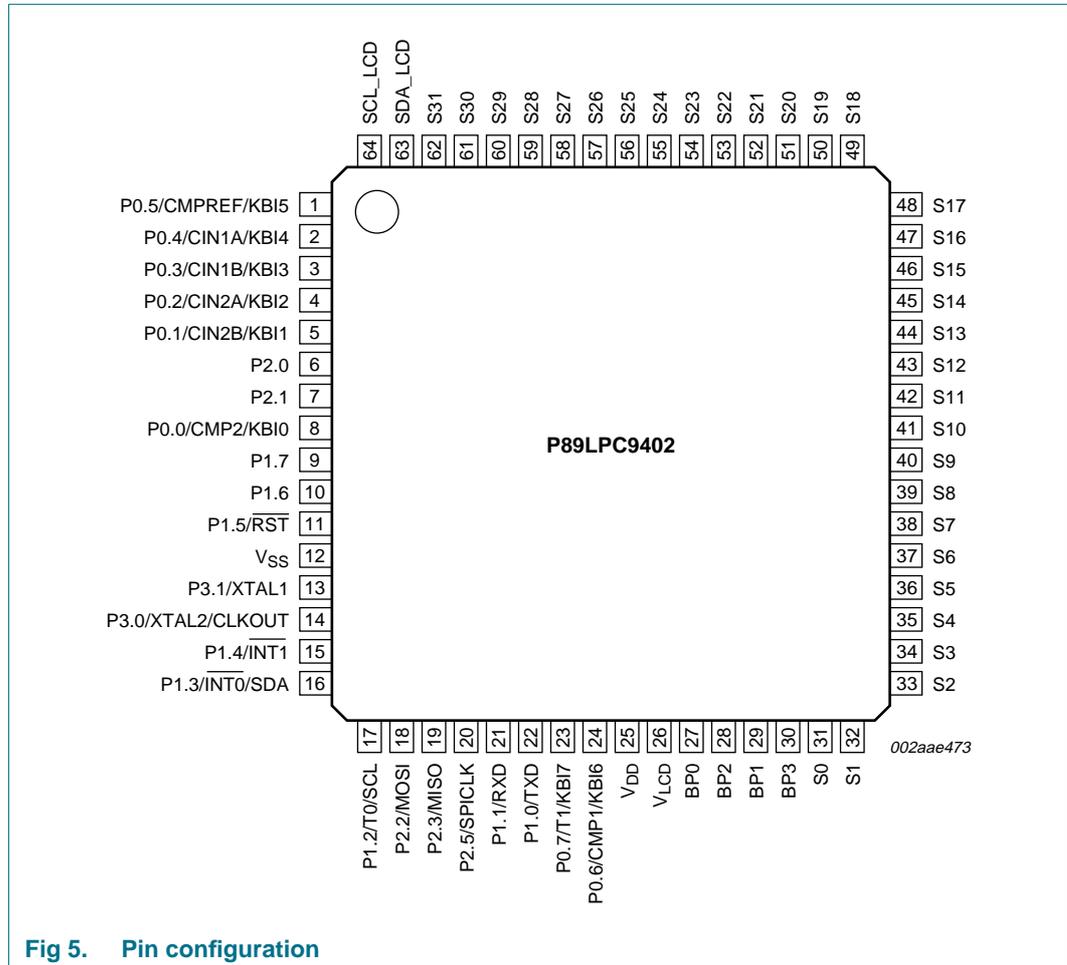


**Fig 5.    Pin configuration**

## 6.2 Pin description

**Table 3.    Pin description**

| Symbol | Pin | Type | Description |
|---|---|---|---|
| P0.0 to P0.7 | | I/O | **Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.14.1 "Port configurations" and Table 12 "Static electrical characteristics" for details. |
| | | | The Keypad Interrupt feature operates with Port 0 pins. |
| | | | All pins have Schmitt trigger inputs. |
| | | | Port 0 also provides various special functions as described below: |
| P0.0/CMP2/ KBI0 | 8 | I/O | **P0.0** — Port 0 bit 0. |
| | | O | **CMP2** — Comparator 2 output |
| | | I | **KBI0** — Keyboard input 0. |

**Table 3.** **Pin description** …continued

| Symbol | Pin | Type | Description |
|---|---|---|---|
| P0.1/CIN2B/ KBI1 | 5 | I/O | **P0.1 —** Port 0 bit 1. |
| | | I | **CIN2B —** Comparator 2 positive input B. |
| | | I | **KBI1 —** Keyboard input 1. |
| P0.2/CIN2A/ KBI2 | 4 | I/O | **P0.2 —** Port 0 bit 2. |
| | | I | **CIN2A —** Comparator 2 positive input A. |
| | | I | **KBI2 —** Keyboard input 2. |
| P0.3/CIN1B/ KBI3 | 3 | I/O | **P0.3 —** Port 0 bit 3. High current source. |
| | | I | **CIN1B —** Comparator 1 positive input B. |
| | | I | **KBI3 —** Keyboard input 3. |
| P0.4/ CIN1A/ KBI4 | 2 | I/O | **P0.4 —** Port 0 bit 4. High current source. |
| | | I | **CIN1A —** Comparator 1 positive input A. |
| | | I | **KBI4 —** Keyboard input 4. |
| P0.5/ CMPREF/ KBI5 | 1 | I/O | **P0.5 —** Port 0 bit 5. High current source. |
| | | I | **CMPREF —** Comparator reference (negative) input. |
| | | I | **KBI5 —** Keyboard input 5. |
| P0.6/CMP1/ KBI6 | 24 | I/O | **P0.6 —** Port 0 bit 6. High current source. |
| | | O | **CMP1 —** Comparator 1 output. |
| | | I | **KBI6 —** Keyboard input 6. |
| P0.7/T1/KBI7 | 23 | I/O | **P0.7 —** Port 0 bit 7. High current source. |
| | | I/O | **T1 —** Timer/counter 1 external count input or overflow output. |
| | | I | **KBI7 —** Keyboard input 7. |
| P1.0 to P1.7 | | I/O, I [1] | **Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.14.1 "Port configurations" and Table 12 "Static electrical characteristics" for details. P1.2 to P1.3 are open-drain when used as outputs. P1.5 is input only. <br><br> All pins have Schmitt trigger inputs. <br><br> Port 1 also provides various special functions as described below: |
| P1.0/TXD | 22 | I/O | **P1.0 —** Port 1 bit 0. |
| | | O | **TXD —** Transmitter output for serial port. |
| P1.1/RXD | 21 | I/O | **P1.1 —** Port 1 bit 1. |
| | | I | **RXD —** Receiver input for serial port. |
| P1.2/T0/SCL | 17 | I/O | **P1.2 —** Port 1 bit 2 (open-drain when used as output). |
| | | I/O | **T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output). |
| | | I/O | **SCL —** I$^2$C-bus serial clock input/output. |
| P1.3/$\overline{\text{INT0}}$/ SDA | 16 | I/O | **P1.3 —** Port 1 bit 3 (open-drain when used as output). |
| | | I | **$\overline{\text{INT0}}$ —** External interrupt 0 input. |
| | | I/O | **SDA —** I$^2$C-bus serial data input/output. |
| P1.4/$\overline{\text{INT1}}$ | 15 | I | **P1.4 —** Port 1 bit 4. High current source. |
| | | I | **$\overline{\text{INT1}}$ —** External interrupt 1 input. |

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**Table 3.      Pin description** …*continued*

| Symbol | Pin | Type | Description |
|---|---|---|---|
| P1.5/$\overline{\text{RST}}$ | 11 | I | **P1.5 —** Port 1 bit 5 (input only). |
| | | I | $\overline{\text{RST}}$ **—** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. |
| P1.6 | 10 | I/O | **P1.6 —** Port 1 bit 6. High current source. |
| P1.7 | 9 | I/O | **P1.7 —** Port 1 bit 7. High current source. |
| P2.0 to P2.3, P2.5 | | I/O | **Port 2:** Port 2 is an 5-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.14.1 "Port configurations" and Table 12 "Static electrical characteristics" for details. |
| | | | All pins have Schmitt trigger inputs. |
| | | | Port 2 also provides various special functions as described below: |
| P2.0 | 6 | I/O | **P2.0 —** Port 2 bit 0. |
| P2.1 | 7 | I/O | **P2.1 —** Port 2 bit 1. |
| P2.2/MOSI | 18 | I/O | **P2.2 —** Port 2 bit 2. |
| | | I/O | **MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input. |
| P2.3/MISO | 19 | I/O | **P2.3 —** Port 2 bit 3. |
| | | I/O | **MISO —** When configured as master, this pin is input, when configured as slave, this pin is output. |
| P2.5/SPICLK | 20 | I/O | **P2.5 —** Port 2 bit 5. |
| | | I/O | **SPICLK —** SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input. |
| P3.0 to P3.1 | | I/O | **Port 3:** Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.14.1 "Port configurations" and Table 12 "Static electrical characteristics" for details. |
| | | | All pins have Schmitt triggered inputs. |
| | | | Port 3 also provides various special functions as described below: |
| P3.0/XTAL2/ CLKOUT | 14 | I/O | **P3.0 —** Port 3 bit 0. |
| | | O | **XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration. |
| | | O | **CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK - TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer. |
| P3.1/XTAL1 | 13 | I/O | **P3.1 —** Port 3 bit 1. |
| | | I | **XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer. |
| SDA_LCD | 63 | I/O | **SDA LCD —** $I^2C$-bus data signal for the LCD controller. |
| SCL_LCD | 64 | I/O | **SCL LCD —** $I^2C$-bus clock signal for the LCD controller. |
| BP0 to BP3 | 27 to 30 | O | **BP0 to BP3:** LCD backplane outputs. |

**Table 3.** **Pin description** *…continued*

| Symbol | Pin | Type | Description |
|--------|-----|------|-------------|
| S0 to S31 | 31 to 62 | O | **S0 to S31:** LCD segment outputs. |
| $V_{SS}$ | 12 | I | **Ground:** 0 V reference. |
| $V_{DD}$ | 25 | I | **Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes. |
| $V_{LCD}$ | 26 | I | **LCD power supply:** LCD voltage. |

[1] Input/output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

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# 7. Functional description

**Remark:** Please refer to the P89LPC9402 *User manual* for a more detailed functional description.

## 7.1 Special function registers

**Remark:** Special Function Registers (SFRs) accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', logic 0 or logic 1 can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with logic 0, but can return any value when read (even if it was written with logic 0). It is a reserved bit and may be used in future derivatives.
  - Logic 0 **must** be written with logic 0, and will return a logic 0 when read.
  - Logic 1 **must** be written with logic 1, and will return a logic 1 when read.

**Table 4.    Special function registers**

*\* indicates SFRs that are bit addressable.*

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MSB | | | | | | | LSB | Hex | Binary |
| | | **Bit address** | **E7** | **E6** | **E5** | **E4** | **E3** | **E2** | **E1** | **E0** | | |
| ACC* | Accumulator | E0H | | | | | | | | | 00 | 0000 0000 |
| AUXR1 | Auxiliary function register | A2H | CLKLP | EBRR | ENT1 | ENT0 | SRST | 0 | - | DPS | 00 | 0000 00x0 |
| | | **Bit address** | **F7** | **F6** | **F5** | **F4** | **F3** | **F2** | **F1** | **F0** | | |
| B* | B register | F0H | | | | | | | | | 00 | 0000 0000 |
| BRGR0[1] | Baud rate generator rate low | BEH | | | | | | | | | 00 | 0000 0000 |
| BRGR1[1] | Baud rate generator rate high | BFH | | | | | | | | | 00 | 0000 0000 |
| BRGCON | Baud rate generator control | BDH | - | - | - | - | - | - | SBRGS | BRGEN | 00[1] | xxxx xx00 |
| CMP1 | Comparator 1 control register | ACH | - | - | CE1 | CP1 | CN1 | OE1 | CO1 | CMF1 | 00[2] | xx00 0000 |
| CMP2 | Comparator 2 control register | ADH | - | - | CE2 | CP2 | CN2 | OE2 | CO2 | CMF2 | 00[2] | xx00 0000 |
| DIVM | CPU clock divide-by-M control | 95H | | | | | | | | | 00 | 0000 0000 |
| DPTR | Data pointer (2 bytes) | | | | | | | | | | | |
| DPH | Data pointer high | 83H | | | | | | | | | 00 | 0000 0000 |
| DPL | Data pointer low | 82H | | | | | | | | | 00 | 0000 0000 |
| FMADRH | Program flash address high | E7H | | | | | | | | | 00 | 0000 0000 |
| FMADRL | Program flash address low | E6H | | | | | | | | | 00 | 0000 0000 |
| FMCON | Program flash control (Read) | E4H | BUSY | - | - | - | HVA | HVE | SV | OI | 70 | 0111 0000 |
| | Program flash control (Write) | E4H | FMCMD.7 | FMCMD.6 | FMCMD.5 | FMCMD.4 | FMCMD.3 | FMCMD.2 | FMCMD.1 | FMCMD.0 | | |
| FMDATA | Program flash data | E5H | | | | | | | | | 00 | 0000 0000 |
| I2ADR | I2C-bus slave address register | DBH | I2ADR.6 | I2ADR.5 | I2ADR.4 | I2ADR.3 | I2ADR.2 | I2ADR.1 | I2ADR.0 | GC | 00 | 0000 0000 |
| | | **Bit address** | **DF** | **DE** | **DD** | **DC** | **DB** | **DA** | **D9** | **D8** | | |
| I2CON* | I2C-bus control register | D8H | - | I2EN | STA | STO | SI | AA | - | CRSEL | 00 | x000 00x0 |
| I2DAT | I2C-bus data register | DAH | | | | | | | | | | |

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NXP Semiconductors

8-bit microcontroller with accelerated two-clock 80C51 core

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**Table 4.    Special function registers** ...continued
*indicates SFRs that are bit addressable.*

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MSB | | | | | | | LSB | Hex | Binary |
| I2SCLH | Serial clock generator/SCL duty cycle register high | DDH | | | | | | | | | 00 | 0000 0000 |
| I2SCLL | Serial clock generator/SCL duty cycle register low | DCH | | | | | | | | | 00 | 0000 0000 |
| I2STAT | I²C-bus status register | D9H | STA.4 | STA.3 | STA.2 | STA.1 | STA.0 | 0 | 0 | 0 | F8 | 1111 1000 |
| | Bit address | | AF | AE | AD | AC | AB | AA | A9 | A8 | | |
| IEN0* | Interrupt enable 0 | A8H | EA | EWDRT | EBO | ES/ESR | ET1 | EX1 | ET0 | EX0 | 00 | 0000 0000 |
| | Bit address | | EF | EE | ED | EC | EB | EA | E9 | E8 | | |
| IEN1* | Interrupt enable 1 | E8H | - | EST | - | - | ESPI | EC | EKBI | EI2C | 00[2] | 00x0 0000 |
| | Bit address | | BF | BE | BD | BC | BB | BA | B9 | B8 | | |
| IP0* | Interrupt priority 0 | B8H | - | PWDRT | PBO | PS/PSR | PT1 | PX1 | PT0 | PX0 | 00[2] | x000 0000 |
| IP0H | Interrupt priority 0 high | B7H | - | PWDRTH | PBOH | PSH/PSRH | PT1H | PX1H | PT0H | PX0H | 00[2] | x000 0000 |
| | Bit address | | FF | FE | FD | FC | FB | FA | F9 | F8 | | |
| IP1* | Interrupt priority 1 | F8H | - | PST | - | - | PSPI | PC | PKBI | PI2C | 00[2] | 00x0 0000 |
| IP1H | Interrupt priority 1 high | F7H | - | PSTH | - | - | PSPIH | PCH | PKBIH | PI2CH | 00[2] | 00x0 0000 |
| KBCON | Keypad control register | 94H | - | - | - | - | - | - | PATN_SEL | KBIF | 00[2] | xxxx xx00 |
| KBMASK | Keypad interrupt mask register | 86H | | | | | | | | | 00 | 0000 0000 |
| KBPATN | Keypad pattern register | 93H | | | | | | | | | FF | 1111 1111 |
| | Bit address | | 87 | 86 | 85 | 84 | 83 | 82 | 81 | 80 | | |
| P0* | Port 0 | 80H | T1/KB7 | CMP1/KB6 | CMPREF/KB5 | CIN1A/KB4 | CIN1B/KB3 | CIN2A/KB2 | CIN2B/KB1 | CMP2/KB0 | | [2] |
| | Bit address | | 97 | 96 | 95 | 94 | 93 | 92 | 91 | 90 | | |
| P1* | Port 1 | 90H | - | - | $\overline{RST}$ | $\overline{INT1}$ | $\overline{INT0}$/SDA | T0/SCL | RXD | TXD | | [2] |
| | Bit address | | 97 | 96 | 95 | 94 | 93 | 92 | 91 | 90 | | |
| P2* | Port 2 | A0H | - | - | SPICLK | $\overline{SS}$ | MISO | MOSI | - | - | | [2] |
| | Bit address | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| P3* | Port 3 | B0H | - | - | - | - | - | - | XTAL1 | XTAL2 | | [2] |

**Table 4.**  **Special function registers** …continued

*indicates SFRs that are bit addressable.*

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|------|-------------|-----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| | | | **MSB** | | | | | | | **LSB** | **Hex** | **Binary** |
| P0M1 | Port 0 output mode 1 | 84H | (P0M1.7) | (P0M1.6) | (P0M1.5) | (P0M1.4) | (P0M1.3) | (P0M1.2) | (P0M1.1) | (P0M1.0) | FF[2] | 1111 1111 |
| P0M2 | Port 0 output mode 2 | 85H | (P0M2.7) | (P0M2.6) | (P0M2.5) | (P0M2.4) | (P0M2.3) | (P0M2.2) | (P0M2.1) | (P0M2.0) | 00[2] | 0000 0000 |
| P1M1 | Port 1 output mode 1 | 91H | (P1M1.7) | (P1M1.6) | - | (P1M1.4) | (P1M1.3) | (P1M1.2) | (P1M1.1) | (P1M1.0) | D3[2] | 11x1 xx11 |
| P1M2 | Port 1 output mode 2 | 92H | (P1M2.7) | (P1M2.6) | - | (P1M2.4) | (P1M2.3) | (P1M2.2) | (P1M2.1) | (P1M2.0) | 00[2] | 00x0 xx00 |
| P2M1 | Port 2 output mode 1 | A4H | (P2M1.7) | (P2M1.6) | (P2M1.5) | (P2M1.4) | (P2M1.3) | (P2M1.2) | (P2M1.1) | (P2M1.0) | FF[2] | 1111 1111 |
| P2M2 | Port 2 output mode 2 | A5H | (P2M2.7) | (P2M2.6) | (P2M2.5) | (P2M2.4) | (P2M2.3) | (P2M2.2) | (P2M2.1) | (P2M2.0) | 00[2] | 0000 0000 |
| P3M1 | Port 3 output mode 1 | B1H | - | - | - | - | - | - | (P3M1.1) | (P3M1.0) | 03[2] | xxxx xx11 |
| P3M2 | Port 3 output mode 2 | B2H | - | - | - | - | - | - | (P3M2.1) | (P3M2.0) | 00[2] | xxxx xx00 |
| PCON | Power control register | 87H | SMOD1 | SMOD0 | - | BOI | GF1 | GF0 | PMOD1 | PMOD0 | 00 | 0000 0000 |
| PCONA | Power control register A | B5H | RTCPD | - | VCPD | - | I2PD | SPPD | SPD | - | 00[2] | 0000 0000 |
| **Bit address** | | | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | | |
| PSW* | Program status word | D0H | CY | AC | F0 | RS1 | RS0 | OV | F1 | P | 00 | 0000 0000 |
| PT0AD | Port 0 digital input disable | F6H | - | - | PT0AD.5 | PT0AD.4 | PT0AD.3 | PT0AD.2 | PT0AD.1 | - | 00 | xx00 000x |
| RSTSRC | Reset source register | DFH | - | BOIF | BOF | POF | R_BK | R_WD | R_SF | R_EX | | [3] |
| RTCCON | Real-time clock control | D1H | RTCF | RTCS1 | RTCS0 | - | - | - | ERTC | RTCEN | 60[2][4] | 011x xx00 |
| RTCH | Real-time clock register high | D2H | | | | | | | | | 00[4] | 0000 0000 |
| RTCL | Real-time clock register low | D3H | | | | | | | | | 00[4] | 0000 0000 |
| SADDR | Serial port address register | A9H | | | | | | | | | 00 | 0000 0000 |
| SADEN | Serial port address enable | B9H | | | | | | | | | 00 | 0000 0000 |
| SBUF | Serial Port data buffer register | 99H | | | | | | | | | xx | xxxx xxxx |
| **Bit address** | | | **9F** | **9E** | **9D** | **9C** | **9B** | **9A** | **99** | **98** | | |
| SCON* | Serial port control | 98H | SM0/FE | SM1 | SM2 | REN | TB8 | RB8 | TI | RI | 00 | 0000 0000 |
| SSTAT | Serial port extended status register | BAH | DBMOD | INTLO | CIDIS | DBISEL | FE | BR | OE | STINT | 00 | 0000 0000 |
| SP | Stack pointer | 81H | | | | | | | | | 07 | 0000 0111 |
| SPCTL | SPI control register | E2H | SSIG | SPEN | DORD | MSTR | CPOL | CPHA | SPR1 | SPR0 | 04 | 0000 0100 |
| SPSTAT | SPI status register | E1H | SPIF | WCOL | - | - | - | - | - | - | 00 | 00xx xxxx |
| SPDAT | SPI data register | E3H | | | | | | | | | 00 | 0000 0000 |

**Table 4.** **Special function registers** …continued
* indicates SFRs that are bit addressable.

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|------|-------------|-----------|-----|-----|-----|-----|-----|-----|-----|-----|------|--------|
| | | | **MSB** | | | | | | | **LSB** | **Hex** | **Binary** |
| TAMOD | Timer 0 and 1 auxiliary mode | 8FH | - | - | - | T1M2 | - | - | - | T0M2 | 00 | xxx0 xxx0 |
| | | **Bit address** | **8F** | **8E** | **8D** | **8C** | **8B** | **8A** | **89** | **88** | | |
| TCON* | Timer 0 and 1 control | 88H | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00 | 0000 0000 |
| TH0 | Timer 0 high | 8CH | | | | | | | | | 00 | 0000 0000 |
| TH1 | Timer 1 high | 8DH | | | | | | | | | 00 | 0000 0000 |
| TL0 | Timer 0 low | 8AH | | | | | | | | | 00 | 0000 0000 |
| TL1 | Timer 1 low | 8BH | | | | | | | | | 00 | 0000 0000 |
| TMOD | Timer 0 and 1 mode | 89H | T1GATE | T1C/T | T1M1 | T1M0 | T0GATE | T0C/T | T0M1 | T0M0 | 00 | 0000 0000 |
| TRIM | Internal oscillator trim register | 96H | RCCLK | ENCLK | TRIM.5 | TRIM.4 | TRIM.3 | TRIM.2 | TRIM.1 | TRIM.0 | | [4] [5] |
| WDCON | Watchdog control register | A7H | PRE2 | PRE1 | PRE0 | - | - | WDRUN | WDTOF | WDCLK | | [4] [6] |
| WDL | Watchdog load | C1H | | | | | | | | | FF | 1111 1111 |
| WFEED1 | Watchdog feed 1 | C2H | | | | | | | | | | |
| WFEED2 | Watchdog feed 2 | C3H | | | | | | | | | | |

[1]  All ports are in input only (high-impedance) state after power-up.

[2]  BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[3]  The RSTSRC register reflects the cause of the P89LPC9402 reset except BOIF bit. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is x011 0000.

[4]  After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[5]  On power-on reset and watchdog reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[6]  The only reset sources that affect these SFRs are power-on reset and watchdog reset.

**Table 5.    Extended special function registers[1]**

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|------|-------------|-----------|------|---|---|---|---|---|---|---|-----|-------|
| | | | **MSB** | | | | | | | **LSB** | **Hex** | **Binary** |
| BODCFG | BOD configuration register | FFC8H | - | - | - | - | - | - | BOICFG1 | BOICFG0 | [2] | |
| CLKCON | CLOCK Control register | FFDEH | CLKOK | - | - | XTALWD | CLKDBL | FOSC2 | FOSC1 | FOSC0 | [3] | |
| RTCDATH | Real-time clock data register high | FFBFH | | | | | | | | | 00 | 0000 0000 |
| RTCDATL | Real-time clock data register low | FFBEH | | | | | | | | | 00 | 0000 0000 |

[1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A,@DPTR and MOVX @DPTR,A instructions are used to access these extended SFRs.

[2] The BOICFG1/0 will be copied from UCFG1.5 and UCFG1.3 when power-on reset.

[3] CLKCON register reset value comes from UCFG1 and UCFG2. The reset value of CLKCON.2 to CLKCON.0 come from UCFG1.2 to UCFG1.0 and reset value of CLKDBL bit comes from UCFG2.7.

## 7.2 Enhanced CPU

The P89LPC9402 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

## 7.3 Clocks

### 7.3.1 Clock definitions

The P89LPC9402 device has several internal clocks as defined below:

**OSCCLK —** Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 6) and can also be optionally divided to a slower frequency (see Section 7.9 "CCLK modification: DIVM register").

**Note:** $f_{osc}$ is defined as the OSCCLK frequency.

**CCLK —** CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

**RCCLK —** The internal 7.373 MHz RC oscillator output. The clock doubler option, when enabled, provides an output frequency of 14.746 MHz.

**PCLK —** Clock for the various peripheral devices and is $^{CCLK}/_2$.

### 7.3.2 CPU clock (OSCCLK)

The P89LPC9402 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source.

### 7.3.3 Crystal oscillator option

The crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 18 MHz. It can be the clock source of OSCCLK, RTC and WDT.

#### 7.3.3.1 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

#### 7.3.3.2 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

#### 7.3.3.3 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration.

### 7.3.4 Clock output

The P89LPC9402 supports a user-selectable clock output function on the XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on XTAL1) and if the RTC and WDT are not using the crystal oscillator as their clock source. This allows external devices to synchronize to the P89LPC9402. This output is enabled by the ENCLK bit in the TRIM register.

The frequency of this clock output is $\frac{1}{2}$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

## 7.4 On-chip RC oscillator option

The P89LPC9402 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory preprogrammed value to adjust the oscillator frequency to 7.373 MHz $\pm$ 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies. When the clock doubler option is enabled (UCFG2.7 = 1), the output frequency is 14.746 MHz. If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to reduce power consumption. On reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower. When clock doubler option is enabled, BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are required to hold the device in reset at power-up until $V_{DD}$ has reached its specified level.

## 7.5 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz, calibrated to $\pm$ 5 % at room temperature. This oscillator can be used to save power when a high clock frequency is not needed.

## 7.6 External clock input option

In this configuration, the processor clock is derived from an external source driving the P3.1/XTAL1 pin. The rate may be from 0 Hz up to 18 MHz. The P3.0/XTAL2 pin may be used as a standard port pin or a clock output. When using an oscillator frequency above 12 MHz, BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are required to hold the device in reset at power-up until $V_{DD}$ has reached its specified level.

## 7.7 Clock sources switch on the fly

P89LPC9402 can implement clock source switch in any sources of watchdog oscillator, 7 MHz/14 MHz IRC oscillator, external clock source (external crystal or external clock input) during code is running. CLKOK bit in CLKCON register is used to indicate the clock switch status. CLKOK is cleared when starting clock source switch and set when completed. Notice that when CLKOK is '0', writing to CLKCON register is not allowed.
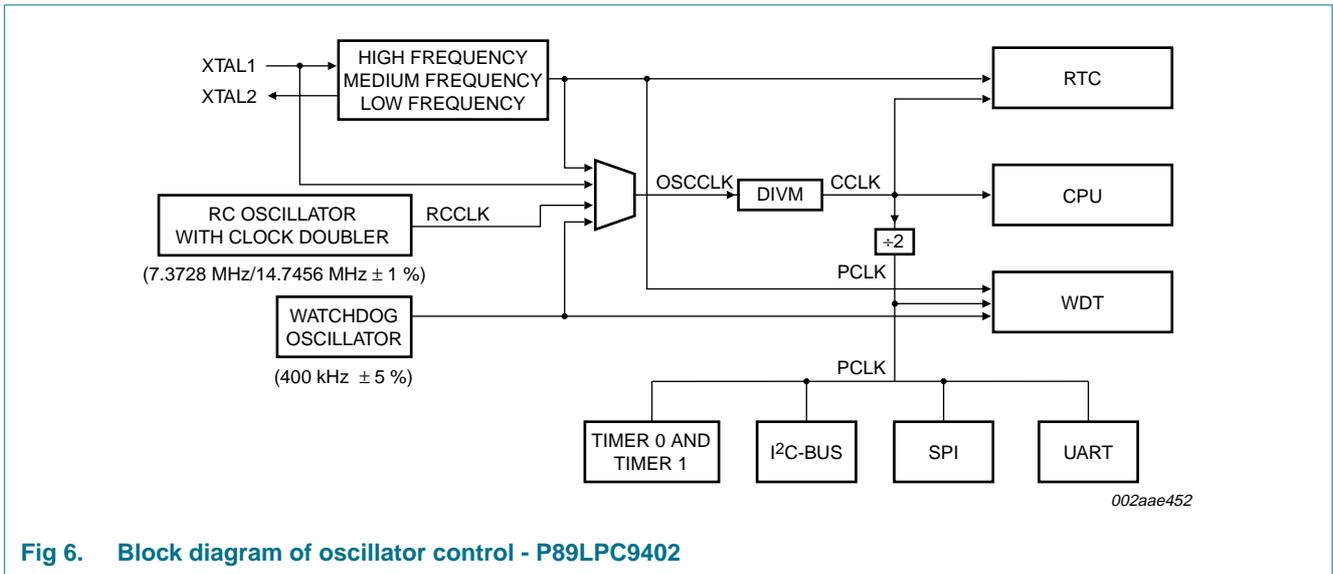
**Fig 6.    Block diagram of oscillator control - P89LPC9402**

## 7.8 CPU Clock (CCLK) wake-up delay

The P89LPC9402 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 1024 OSCCLK cycles plus 60 µs to 100 µs. If the clock source is the internal RC oscillator, the delay is 200 µs to 300 µs. If the clock source is watchdog oscillator or external clock, the delay is 32 OSCCLK cycles.

## 7.9 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

## 7.10 Low power select

The P89LPC9402 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

## 7.11 Memory organization

The various P89LPC9402 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.

- IDATA

  Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC9402 has 8 kB of on-chip Code memory.

## 7.12 Data RAM arrangement

The 768 bytes of on-chip RAM are organized as shown in Table 6.

**Table 6.** **On-chip data memory usages**

| Type | Data RAM | Size (bytes) |
|------|----------|--------------|
| DATA | Memory that can be addressed directly and indirectly | 128 |
| IDATA | Memory that can be addressed indirectly | 256 |

## 7.13 Interrupts

The P89LPC9402 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC9402 supports 13 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port TX, serial port RX, combined serial port RX/TX, brownout detect, watchdog/RTC, $I^2C$-bus, keyboard, comparators 1 and 2, SPI.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1 and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

### 7.13.1 External interrupt inputs

The P89LPC9402 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC9402 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 7.16 "Power reduction modes" for details.
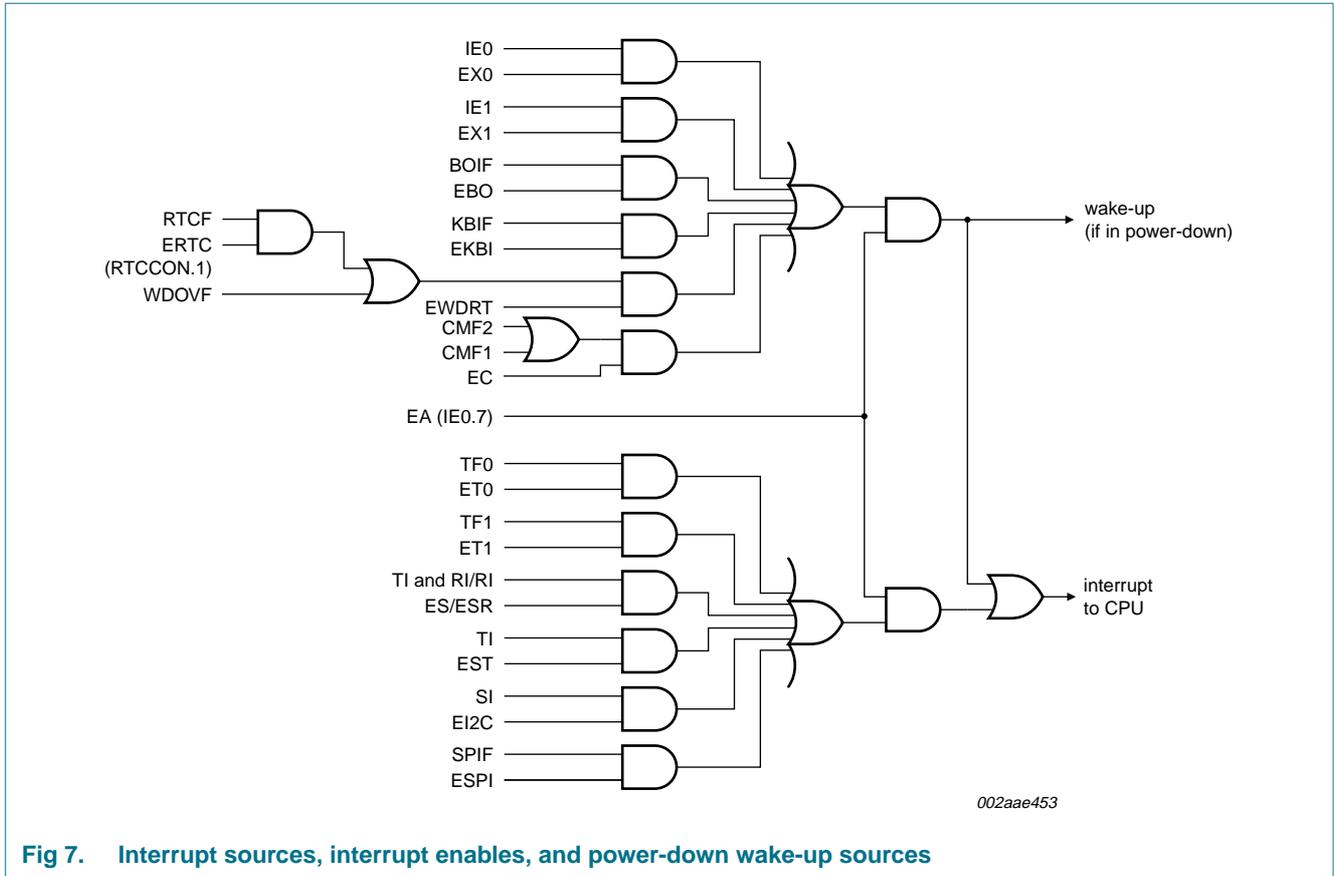
**Fig 7.    Interrupt sources, interrupt enables, and power-down wake-up sources**

### 7.14  I/O ports

The P89LPC9402 has four I/O ports: Port 0 and Port 1 are 8-bit ports. Port 2 is a 5-bit port. Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options chosen, as shown in Table 7.

**Table 7.    Number of I/O pins available**

| Clock source | Reset option | Number of I/O pins (not including LCD pins) |
|---|---|---|
| On-chip oscillator or watchdog oscillator | No external reset (except during power-up) | 23 |
| | External $\overline{RST}$ pin supported | 22 |
| External clock input | No external reset (except during power-up) | 22 |
| | External $\overline{RST}$ pin supported[1] | 21 |
| Low/medium/high speed oscillator (external crystal or resonator) | No external reset (except during power-up) | 21 |
| | External $\overline{RST}$ pin supported[1] | 20 |

[1]    Required for operation above 12 MHz.

### 7.14.1  Port configurations

All but three I/O port pins on the P89LPC9402 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open-drain, and input-only. Two configuration registers for each port select the output type for each port pin.

1. P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.

2. P1.2 (SCL/T0) and P1.3 (SDA/$\overline{\text{INT0}}$) may only be configured to be either input-only or open-drain.

#### 7.14.1.1  Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC9402 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to $V_{DD}$, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt trigger input that also has a glitch suppression circuit.

#### 7.14.1.2  Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to $V_{DD}$.

An open-drain port pin has a Schmitt trigger input that also has a glitch suppression circuit.

#### 7.14.1.3  Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt trigger input that also has a glitch suppression circuit.

#### 7.14.1.4  Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt trigger input that also has a glitch suppression circuit.The P89LPC9402 device has high current source on eight pins in push-pull mode. See Table 11 "Limiting values".

### 7.14.2  Port 0 analog functions

The P89LPC9402 incorporates two analog comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to logic 0s to enable digital functions.

### 7.14.3 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 and are configurable for either input-only or open-drain.

Every output on the P89LPC9402 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 12 "Static electrical characteristics" for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

## 7.15 Power monitoring functions

The P89LPC9402 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on detect and brownout detect.

### 7.15.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. Enhanced brownout detection has 3 independent functions: BOD reset, BOD interrupt and BOD FLASH.

BOD reset is always on except in total Power-down mode. It could not be disabled in software. BOD interrupt may be enabled or disabled in software. BOD FLASH is always on, except in Power-down modes and could not be disabled in software.

BOD reset and BOD interrupt, each has four trip voltage levels. BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are used as trip point configuration bits of BOD reset. BOICFG1 bit and BOICFG0 bit in register BODCFG are used as trip point configuration bits of BOD interrupt. BOD reset voltage should be lower than BOD interrupt trip point. BOD FLASH is used for flash programming/erase protection and has only 1 trip voltage of 2.4 V. Please refer to P89LPC9402 *User manual* for detail configurations.

If brownout detection is enabled the brownout condition occurs when $V_{DD}$ falls below the brownout trip voltage and is negated when $V_{DD}$ rises above the brownout trip voltage.

For correct activation of brownout detect, the $V_{DD}$ rise and fall times must be observed. Please see Table 12 "Static electrical characteristics" for specifications.

### 7.15.2 Power-on detection

The Power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

## 7.16 Power reduction modes

The P89LPC9402 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

### 7.16.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

### 7.16.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC9402 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the data retention voltage $V_{DDR}$. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after $V_{DD}$ has been lowered to $V_{DDR}$, therefore it is highly recommended to wake-up the processor via reset in this case. $V_{DD}$ must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: Brownout detect, watchdog timer, Comparators (note that Comparators can be powered-down separately), and RTC/System Timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

### 7.16.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

## 7.17 Reset

The P1.5/$\overline{RST}$ pin can function as either a LOW-active reset input or as a digital input, P1.5. The Reset Pin Enable (RPE) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

**Remark:** During a power-up sequence, the RPE selection is overridden and this pin always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this pin will function as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

**Note:** During a power cycle, $V_{DD}$ must fall below $V_{POR}$ before power is reapplied, in order to ensure a power-on reset (see Table 12 "Static electrical characteristics").

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1)
- Power-on detect
- Brownout detect
- Watchdog timer
- Software reset
- UART break character detect reset

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- A Watchdog reset is similar to a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

### 7.17.1 Reset vector

Following reset, the P89LPC9402 will fetch instructions from either address 0000H or the Boot address. The Boot address is formed by using the Boot Vector as the high byte of the address and the low byte of the address = 00H.

The Boot address will be used if a UART break reset occurs, or the non-volatile Boot Status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see P89LPC9402 *User manual*). Otherwise, instructions will be fetched from address 0000H.

## 7.18 Timers/counters 0 and 1

The P89LPC9402 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counter. An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'Timer' function, the register is incremented every machine cycle.

In the 'Counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

### 7.18.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

### 7.18.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

### 7.18.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

### 7.18.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

### 7.18.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

### 7.18.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

## 7.19 RTC/system timer

The P89LPC9402 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator. Only power-on reset and watchdog reset will reset the RTC and its associated SFRs to the default state.

The 16-bit loadable counter portion of the RTC is readable by reading the RTCDATL and RTCDATH registers.

## 7.20 UART

The P89LPC9402 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC9402 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

### 7.20.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $\frac{1}{16}$ of the CPU clock frequency.

### 7.20.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 7.20.5 "Baud rate generator and selection").

### 7.20.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable $9^{th}$ data bit, and a stop bit (logic 1). When data is transmitted, the $9^{th}$ data bit (TB8 in SCON) can be assigned the value of logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the $9^{th}$ data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either $\frac{1}{16}$ or $\frac{1}{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

### 7.20.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable $9^{th}$ data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 7.20.5 "Baud rate generator and selection").

### 7.20.5 Baud rate generator and selection

The P89LPC9402 enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 8). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent Baud Rate Generator uses OSCCLK.
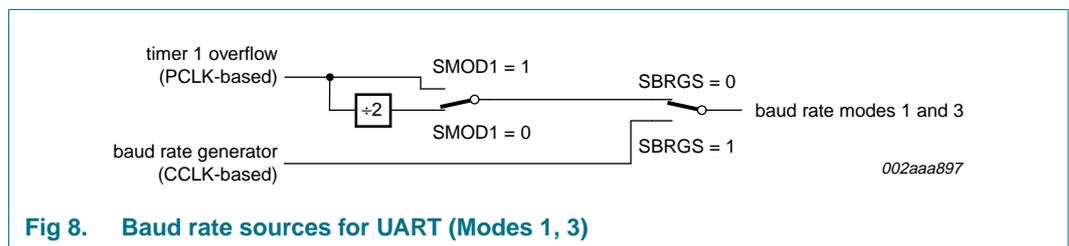


**Fig 8. Baud rate sources for UART (Modes 1, 3)**

### 7.20.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is logic 1, framing errors can be made available in SCON.7 respectively. If SMOD0 is logic 0, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is logic 0.

### 7.20.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

### 7.20.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

### 7.20.9 Transmit interrupts with double buffering enabled (modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the TX interrupt is generated when the double buffer is ready to receive new data.

### 7.20.10 The 9th bit (bit 8) in double buffering (modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the TX interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

### 7.21 I²C-bus serial interface

The I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves

- Multi master bus (no central master)

- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus

- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus

- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer

- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in Figure 9. The P89LPC9402 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.
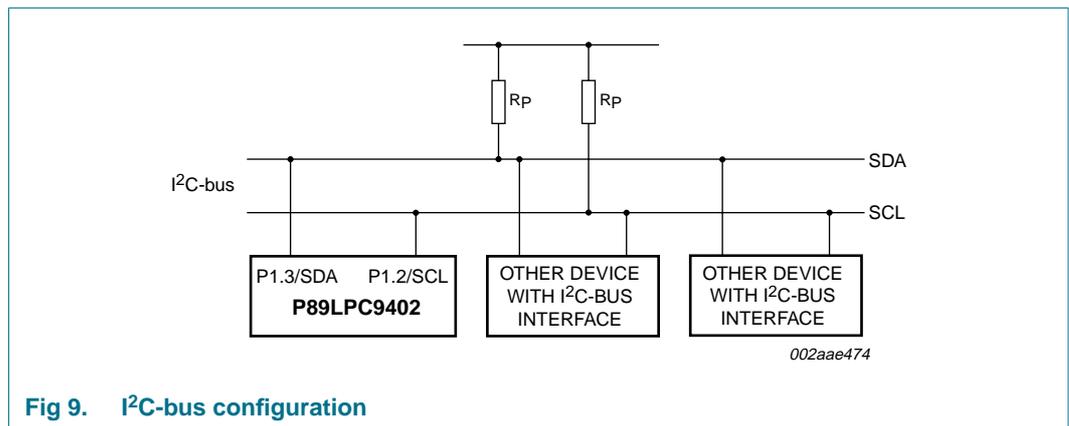


**Fig 9.  I²C-bus configuration**
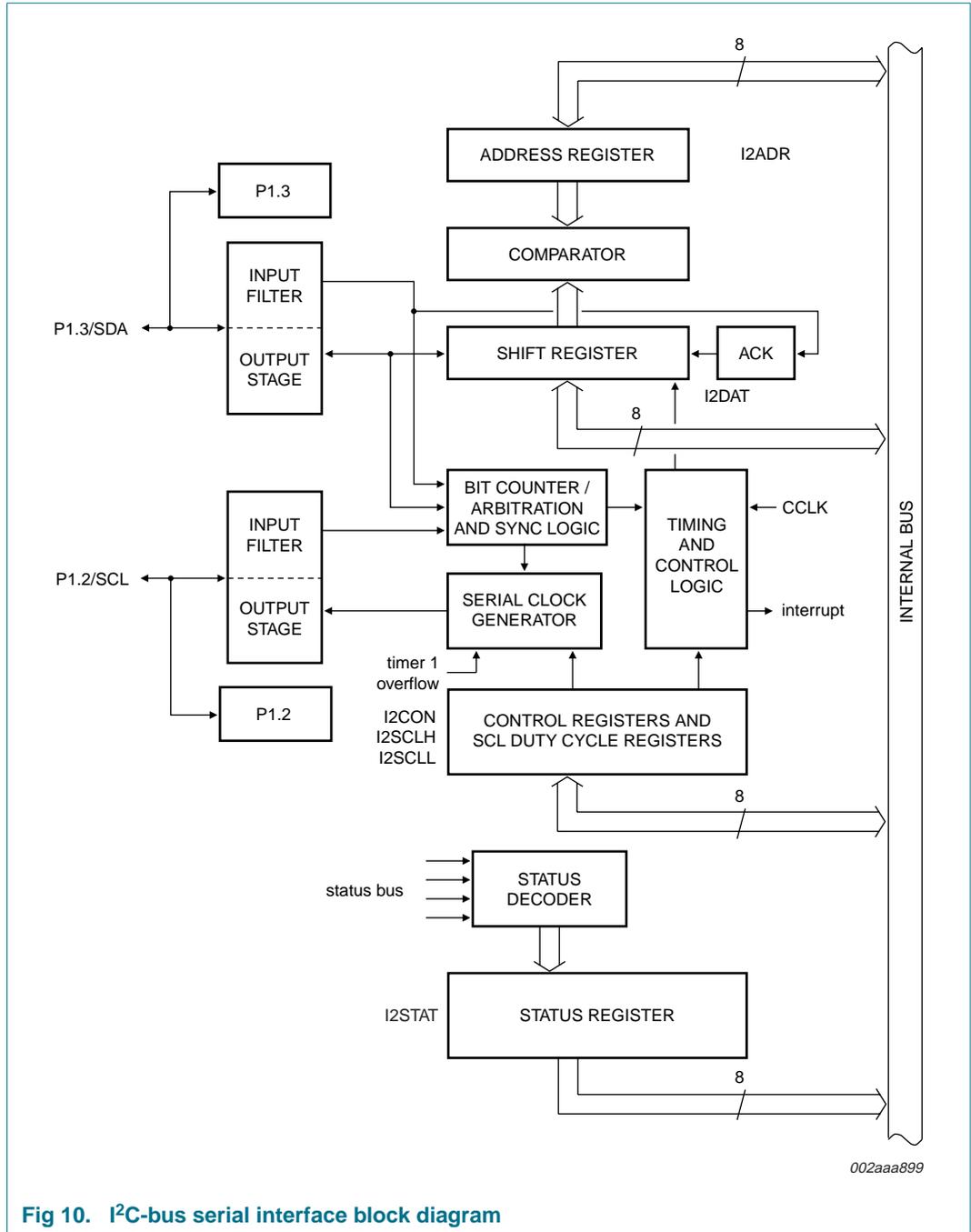
**Fig 10. I²C-bus serial interface block diagram**

## 7.22 SPI

The P89LPC9402 provides another high-speed serial communication interface, the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 4.5 Mbit/s can be supported in Master mode or up to 3 Mbit/s in Slave mode. It has a transfer completion flag and write collision flag protection.
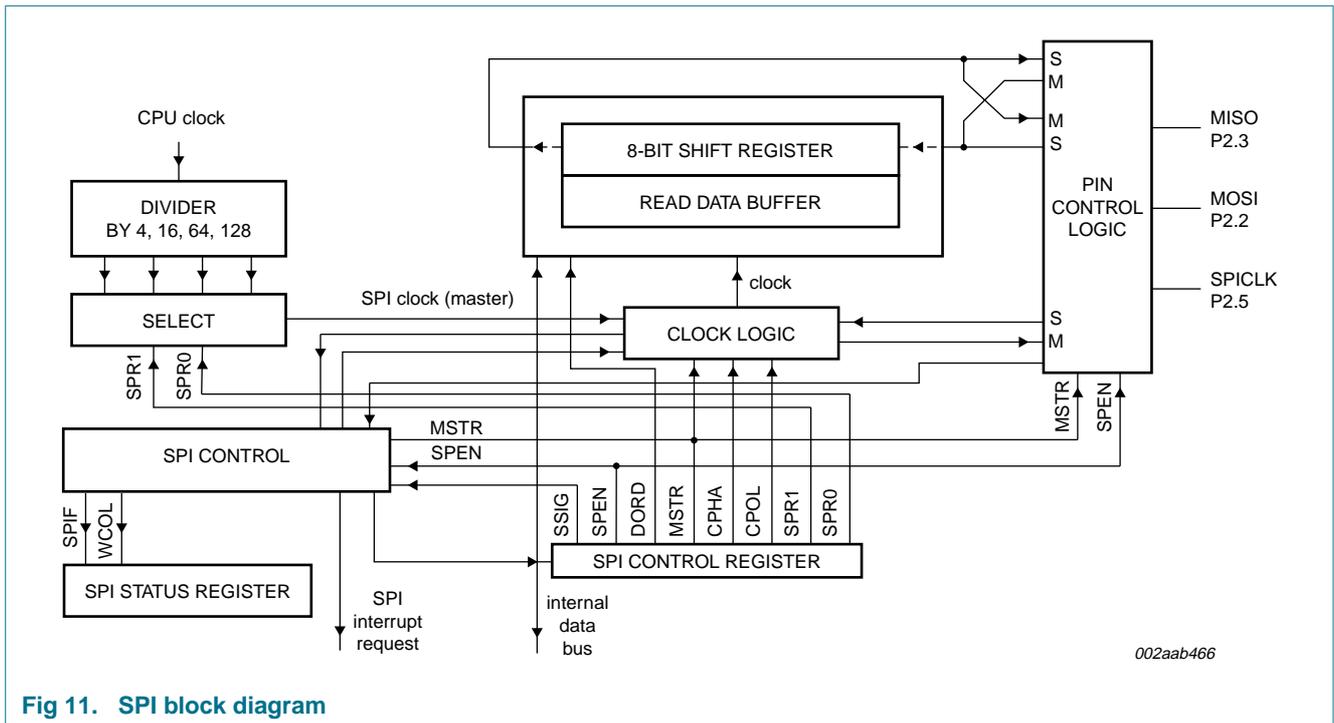


**Fig 11.  SPI block diagram**

The SPI interface has three pins: SPICLK, MOSI, MISO and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the master mode and is input in the slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.

Typical connections are shown in Figure 12 through Figure 14.

### 7.22.1 Typical SPI configurations
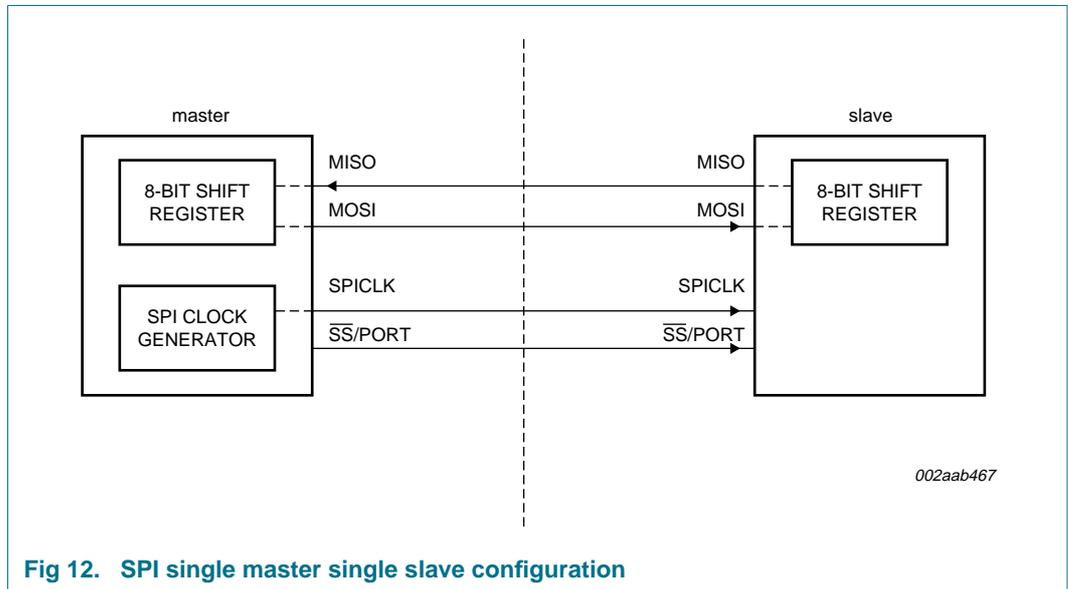


**Fig 12.** SPI single master single slave configuration
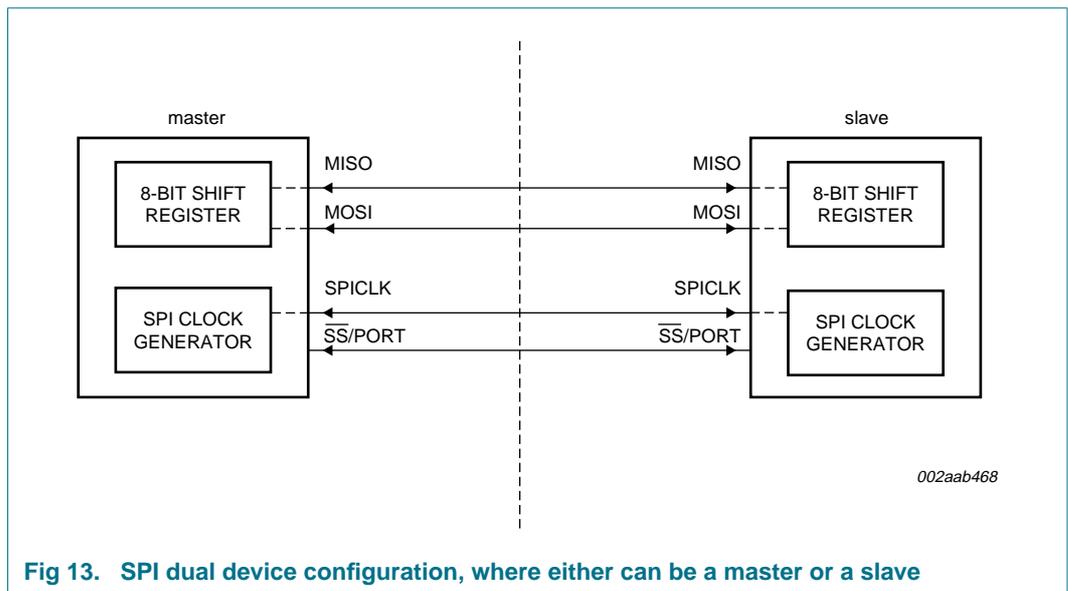


**Fig 13.** SPI dual device configuration, where either can be a master or a slave
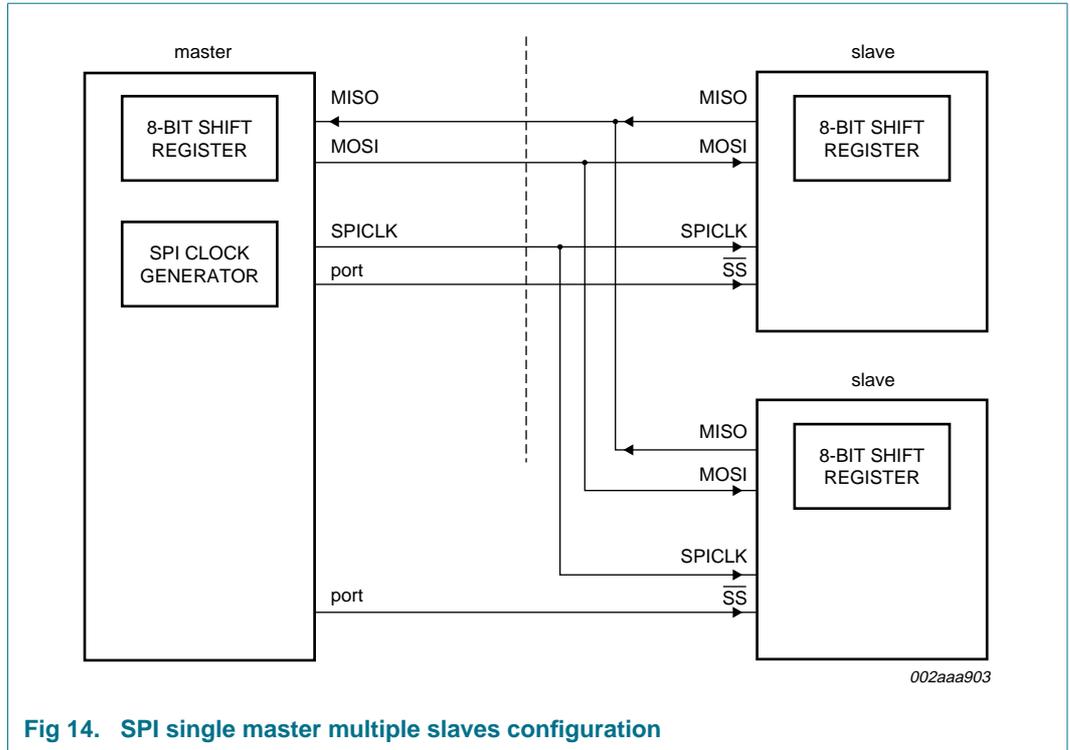
**Fig 14. SPI single master multiple slaves configuration**

## 7.23 Analog comparators

Two analog comparators are provided on the P89LPC9402. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logic 1 (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

The overall connections to both comparators are shown in Figure 15. The comparators function to $V_{DD}$ = 2.4 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 μs. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.
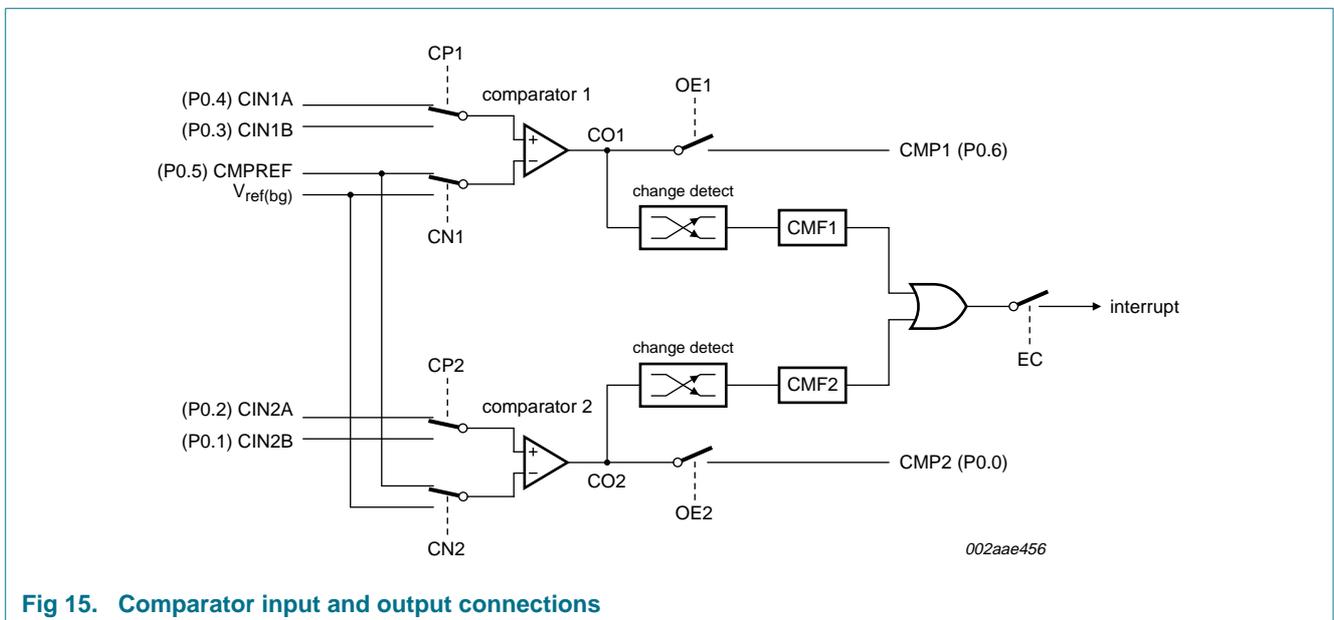


**Fig 15.  Comparator input and output connections**

### 7.23.1  Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as $V_{ref(bg)}$, is 1.23 V ± 10 %.

### 7.23.2  Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

### 7.23.3  Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake-up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the **oscillator** stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

## 7.24 Keypad interrupt

The Keypad Interrupt (KBI) function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake-up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

## 7.25 Watchdog timer

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler can be the PCLK, the nominal 400 kHz watchdog oscillator or crystal oscillator. The watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 16 shows the watchdog timer in Watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered down, the watchdog is disabled. The watchdog timer has a time-out period that ranges from a few μs to a few seconds. Please refer to the P89LPC9402 *User manual* for more details.
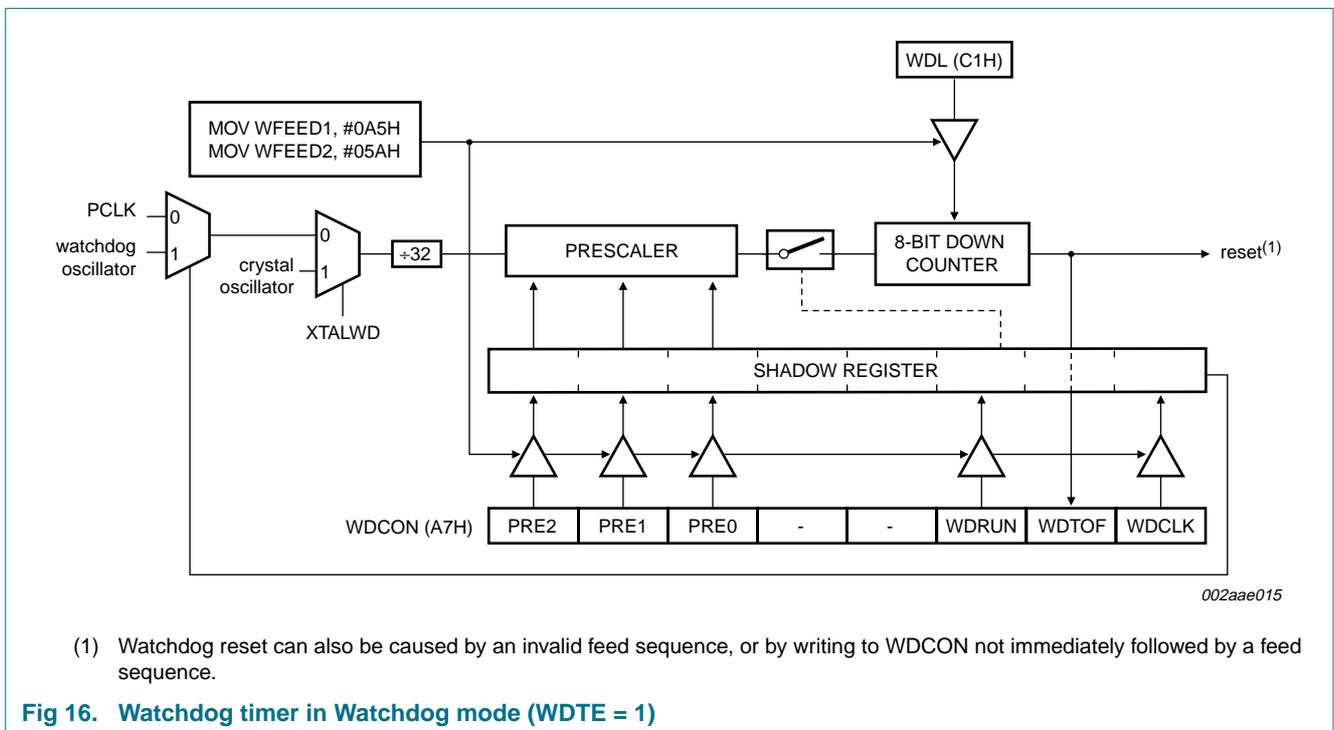


(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

**Fig 16. Watchdog timer in Watchdog mode (WDTE = 1)**

## 7.26 Additional features

### 7.26.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

### 7.26.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

### 7.27 LCD driver

#### 7.27.1 General description

The LCD segment driver in the P89LPC9402 can interface to most LCDs using low multiplex rates. It generates the drive signals for static or multiplexed LCDs containing up to four backplanes and up to 32 segments. The LCD controller communicates to a host using the I$^2$C-bus. The I$^2$C-bus clock and data signals for both the microcontroller and the LCD driver are available on the P89LPC9402 providing system flexibility. Communication overhead to manage the display is minimized by an on-chip display RAM with auto-increment addressing, hardware subaddressing, and display memory switching (static and duplex drive modes).

#### 7.27.2 Functional description

The LCD controller is a versatile peripheral device designed to interface microcontrollers to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 32 segments. The display configurations possible with the LCD controller depend on the number of active backplane outputs required. A selection of display configurations is shown in Table 8. All of these configurations can be implemented in a typical system.

The microcontroller communicates to the LCD controller using the I$^2$C-bus. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies ($V_{DD}$, $V_{SS}$ and $V_{LCD}$) and the LCD panel chosen for the application.

**Table 8.    Selection of display configurations**

| Number of | | 7-segments numeric | | 14- segments alphanumeric | | Dot matrix |
|---|---|---|---|---|---|---|
| Backplanes | Segments | Digits | Indicator symbols | Characters | Indicator symbols | |
| 4 | 128 | 16 | 16 | 8 | 16 | 128 |
| 3 | 96 | 12 | 12 | 6 | 12 | 96 |
| 2 | 64 | 8 | 8 | 4 | 8 | 64 |
| 1 | 32 | 4 | 4 | 2 | 4 | 32 |

#### 7.27.3 LCD bias voltages

LCD biasing voltages are obtained from an internal voltage divider consisting of three series resistors connected between $V_{LCD}$ and $V_{SS}$. The LCD voltage can be temperature compensated externally via the supply to pin $V_{LCD}$. A voltage selector drives the multiplexing of the LCD based on programmable configurations.

#### 7.27.4 Oscillator

#### 7.27.4.1 Internal clock

An internal oscillator provides the clock signals for the internal logic of the LCD controller and its LCD drive signals. After power-up, pin SDA must be HIGH to guarantee that the clock starts.

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### 7.27.5 Timing

The LCD controller timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock.

Frame frequency = $f_{osc(LCD)}$/24.

### 7.27.6 Display register

A display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs, and each column of the display RAM.

### 7.27.7 Segment outputs

The LCD drive section includes 32 segment outputs S0 to S31. The segment output signals are generated according to the multiplexed backplane signals and the display latch data. When less than 32 segment outputs are required, the unused segment outputs should be left open-circuit.

### 7.27.8 Backplane outputs

The LCD drive section has four backplane outputs BP0 to BP3. The backplane output signals are generated in based on the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit. In the 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1:2 multiplex drive mode, BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

### 7.27.9 Display RAM

The display RAM is a static $32 \times 4$-bit RAM which stores LCD data. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 32 segments for backplane 0 (BP0). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

### 7.27.10 Data pointer

The Display RAM is addressed using the data pointer. Either a single byte or a series of display bytes may be loaded into any location of the display RAM.

### 7.27.11 Output bank selector

The LCD controller includes a RAM bank switching feature in the static and 1:2 drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In 1:2 mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This allows display information to be prepared in an alternative bank and then selected for display when it is assembled.

### 7.27.12 Input bank selector

The input bank selector loads display data into the display RAM based on the selected LCD drive configuration. The BANK SELECT command can be used to load display data in bit 2 in static drive mode or in bits 2 and 3 in 1:2 mode. The input bank selector functions are independent of the output bank selector.

### 7.27.13 Blinker

The LCD controller has a very versatile display blinking capability. The whole display can blink at a frequency selected by the BLINK command. Each blink frequency is a multiple integer value of the clock frequency; the ratio between the clock frequency and blink frequency depends on the blink mode selected, as shown in Table 9.

An additional feature allows an arbitrary selection of LCD segments to be blinked in the static and 1:2 drive modes. This is implemented without any communication overheads by the output bank selector which alternates the displayed data between the data in the display RAM bank and the data in an alternative RAM bank at the blink frequency. This mode can also be implemented by the BLINK command.

The entire display can be blinked at a frequency other than the nominal blink frequency by sequentially resetting and setting the display enable bit E at the required rate using the MODE SET command.

**Table 9.    Blinking frequencies**

| Blink mode | Normal operating mode ratio | Normal blink frequency |
|---|---|---|
| Off | - | Blinking off |
| 2 Hz | $f_{osc(LCD)}/768$ | 2 Hz |
| 1 Hz | $f_{osc(LCD)}/1536$ | 1 Hz |
| 0.5 Hz | $f_{osc(LCD)}/3072$ | 0.5 Hz |

Blink modes 0.5 Hz, 1 Hz and 2 Hz, and nominal blink frequencies 0.5 Hz, 1 Hz and 2 Hz correspond to an oscillator frequency ($f_{osc(LCD)}$) of 1536 Hz at pin CLK. The oscillator frequency range is 397 Hz to 3046 Hz.

#### 7.27.13.1 I$^2$C-bus controller

The LCD controller acts as an I$^2$C-bus slave receiver. In the P89LPC9402 the hardware subaddress inputs A0, A,1 and A2 are tied to $V_{SS}$ setting the hardware subaddress = 0.

### 7.27.14 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

### 7.27.15 I$^2$C-bus slave addresses

The I$^2$C-bus slave address is 0111 0000. The LCD controller is a write-only device and will not respond to a read access.

## 7.28 Flash program memory

### 7.28.1 General description

The P89LPC9402 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC9402 flash reliably stores memory contents even after 100,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC9402 uses $V_{DD}$ as the supply voltage to perform the Program/Erase algorithms. When voltage supply is lower than 2.4 V, the BOD FLASH is tripped and flash erase/program is blocked.

### 7.28.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ISP/IAP/ICP.
- Internal fixed boot ROM, containing low-level IAP routines available to user code.
- Default loader providing ISP via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Any flash program or erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- 100,000 typical erase/program cycles for each byte.
- 10 year minimum data retention.

### 7.28.3 Flash organization

The program memory consists of eight 1 kB sectors on the P89LPC9402 device. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 byte to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

### 7.28.4 Using flash as data storage

The flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

### 7.28.5  Flash programming and erasing

Four different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock - serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing for the device to be programmed in circuit through the serial port. The flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit CRC result on either a sector or the entire user code space.

Remark: When voltage supply is lower than 2.4 V, the BOD FLASH is tripped and flash erase/program is blocked.

### 7.28.6  In-circuit programming

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC9402 through a two-wire serial interface. Using commercially available programmers, the NXP ICP facility has made ICP in an embedded application possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC9402 *User manual*.

### 7.28.7  In-application programming

IAP is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The NXP IAP has made IAP in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a Boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF03H. The Boot ROM occupies the program memory space at the top of the address space from FF00H to FEFFH, thereby not conflicting with the user program memory space.

In addition, IAP operations can be accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC9402 *User manual*.

### 7.28.8  In-system programming

ISP is performed without removing the microcontroller from the system. The ISP facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC9402 through the serial port. This firmware is provided by NXP and embedded within each P89LPC9402 device. The NXP ISP facility has made ISP in an embedded application possible with a minimum of additional expense

in components and circuit board area. The ISP function uses five pins ($V_{DD}$, $V_{SS}$, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

### 7.28.9 Power-on reset code execution

The P89LPC9402 contains two special flash elements: the Boot Vector and the Boot Status bit. Following reset, the P89LPC9402 examines the contents of the Boot Status bit. If the Boot Status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status bit is set to a value other than zero, the contents of the Boot Vector are used as the high byte of the execution address and the low byte is set to 00H.

Table 10 shows the factory default Boot Vector setting for these devices. A factory-provided bootloader is pre-programmed into the address space indicated and uses the indicated bootloader entry point to perform ISP functions. This code can be erased by the user.

**Remark:** Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector that contains this bootloader. Instead, the page erase function can be used to erase the first eight 64-byte pages located in this sector.

A custom bootloader can be written with the Boot Vector set to the custom bootloader, if desired.

**Table 10.     Default Boot Vector values and ISP entry points**

| Device | Default Boot Vector | Default boot loader entry point | Default boot loader code range | 1 kB sector range |
|---|---|---|---|---|
| P89LPC9402 | 1FH | 1F00H | 1E00H to 1FFFH | 1C00H to 1FFFH |

### 7.28.10 Hardware activation of the bootloader

The bootloader can also be executed by forcing the device into ISP mode during a power-on sequence (see the P89LPC9402 *User manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the Boot Vector (1FH) is changed, it will no longer point to the factory preprogrammed ISP bootloader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

## 7.29 User configuration bytes

Some user-configurable features of the P89LPC9402 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1 and UCFG2. Please see the P89LPC9402 *User Manual* for additional details.

## 7.30 User sector security bytes

There are eight User Sector Security Bytes on the P89LPC9402 device. Each byte corresponds to one sector. Please see the P89LPC9402 *User manual* for additional details.

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# 8. Limiting values

**Table 11. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*[1]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{amb(bias)}$ | bias ambient temperature | | −55 | +125 | °C |
| $T_{stg}$ | storage temperature | | −65 | +150 | °C |
| $I_{OH(I/O)}$ | HIGH-level output current per input/output pin | | - | 20 | mA |
| $I_{OL(I/O)}$ | LOW-level output current per input/output pin | | - | 20 | mA |
| $I_{I/Otot(max)}$ | maximum total input/output current | | - | 100 | mA |
| $V_n$ | voltage on any other pin | except $V_{SS}$, with respect to $V_{DD}$ | - | 3.5 | V |
| $P_{tot(pack)}$ | total power dissipation (per package) | based on package heat transfer, not device power consumption | - | 1.5 | W |

[1] The following applies to Table 11:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.

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## 9. Static characteristics

**Table 12. Static electrical characteristics**
$V_{DD}$ = 2.4 V to 3.6 V unless otherwise specified.
$T_{amb}$ = −40 °C to +85 °C for industrial applications, unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD(oper)}$ | operating supply current | $V_{DD}$ = 3.6 V; $f_{osc}$ = 12 MHz | [2] | - | 11 | 15 | mA |
| | | $V_{DD}$ = 3.6 V; $f_{osc}$ = 18 MHz | [2] | - | 17 | 23 | mA |
| $I_{DD(idle)}$ | Idle mode supply current | $V_{DD}$ = 3.6 V; $f_{osc}$ = 12 MHz | [2] | - | 3.7 | 5 | mA |
| | | $V_{DD}$ = 3.6 V; $f_{osc}$ = 18 MHz | [2] | - | 6 | 8 | mA |
| $I_{DD(pd)}$ | Power-down mode supply current | $V_{DD}$ = 3.6 V; voltage comparators powered down | [2] | - | 60 | 85 | μA |
| $I_{DD(tpd)}$ | total Power-down mode supply current | $V_{DD}$ = 3.6 V | [3] | - | 9 | 25 | μA |
| $(dV/dt)_r$ | rise rate | of $V_{DD}$ | | - | - | 2 | mV/μs |
| $V_{DDR}$ | data retention supply voltage | | | 1.5 | - | - | V |
| $V_{th(HL)}$ | HIGH-LOW threshold voltage | except SCL, SDA | | $0.22V_{DD}$ | $0.4V_{DD}$ | - | V |
| $V_{IL}$ | LOW-level input voltage | SCL, SDA only | | −0.5 | - | $0.3V_{DD}$ | V |
| $V_{th(LH)}$ | LOW-HIGH threshold voltage | except SCL, SDA | | - | $0.6V_{DD}$ | $0.7V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | SCL, SDA only | | $0.7V_{DD}$ | - | 5.5 | V |
| $V_{hys}$ | hysteresis voltage | port 1 | | - | $0.2V_{DD}$ | - | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 20 mA; $V_{DD}$ = 2.4 V to 3.6 V, all ports, all modes except high-Z | [4] | - | 0.6 | 1.0 | V |
| | | $I_{OL}$ = 3.2 mA; $V_{DD}$ = 2.4 V to 3.6 V; all ports; all modes except high-Z | [4] | - | 0.2 | 0.3 | V |
| $V_{OH}$ | HIGH-level output voltage | $I_{OH}$ = −20 μA; $V_{DD}$ = 2.4 V to 3.6 V; all ports; quasi-bidirectional mode | | $V_{DD} - 0.3$ | $V_{DD} - 0.2$ | - | V |
| | | $I_{OH}$ = −3.2 mA; $V_{DD}$ = 2.4 V to 3.6 V; all ports; push-pull mode | | $V_{DD} - 0.7$ | $V_{DD} - 0.4$ | - | V |
| $V_{xtal}$ | crystal voltage | with respect to $V_{SS}$ | | −0.5 | - | +4.0 | V |
| $V_n$ | voltage on any other pin | except XTAL1, XTAL2, $V_{DD}$, with respect to $V_{SS}$ | | −0.5 | - | +5.5 | V |
| $C_{iss}$ | input capacitance | | [5] | - | - | 15 | pF |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0.4 V | [6] | - | - | −80 | μA |
| $I_{LI}$ | input leakage current | $V_I$ = $V_{IL}$, $V_{IH}$ or $V_{th(HL)}$ | [7] | - | - | ±10 | μA |
| $I_{THL}$ | HIGH-LOW transition current | all ports, $V_I$ = 1.5 V at $V_{DD}$ = 3.6 V | [8] | −30 | - | −450 | μA |
| $R_{RST\_N(int)}$ | internal pull-up resistance on pin $\overline{RST}$ | | | 10 | - | 30 | kΩ |

**Table 12.    Static electrical characteristics** *…continued*

$V_{DD}$ = 2.4 V to 3.6 V unless otherwise specified.

$T_{amb}$ = −40 °C to +85 °C for industrial applications, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{bo}$ | brownout trip voltage | 2.4 V < $V_{DD}$ < 3.6 V; with BOV = 1, BOPD = 0 | 2.40 | - | 2.70 | V |
| $V_{ref(bg)}$ | band gap reference voltage | | 1.11 | 1.23 | 1.34 | V |
| $TC_{bg}$ | band gap temperature coefficient | | - | 10 | 20 | ppm/°C |

[1]    Typical ratings are not guaranteed. The values listed are at room temperature, $V_{DD}$ = 3 V.

[2]    The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3]    The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4]    See Section 8 "Limiting values" on page 44 for steady state (non-transient) limits on $I_{OL}$ or $I_{OH}$. If $I_{OL}/I_{OH}$ exceeds the test condition, $V_{OL}/V_{OH}$ may exceed the related specification.

[5]    Pin capacitance is characterized but not tested.

[6]    Measured with port in quasi-bidirectional mode.

[7]    Measured with port in high-impedance mode.

[8]    Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when $V_I$ is approximately 2 V.

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## 10. Dynamic characteristics

**Table 13.  Dynamic characteristics (12 MHz)**

*$V_{DD}$ = 2.4 V to 3.6 V unless otherwise specified.*
*$T_{amb}$ = −40 °C to +85 °C for industrial applications, unless otherwise specified.*[1][2]

| Symbol | Parameter | Conditions | Variable clock | | $f_{osc}$ = 12 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | **Min** | **Max** | **Min** | **Max** | |
| $f_{osc(RC)}$ | internal RC oscillator frequency | | 7.189 | 7.557 | 7.189 | 7.557 | MHz |
| $f_{osc(WD)}$ | internal watchdog oscillator frequency | | 320 | 520 | 320 | 520 | kHz |
| $f_{osc}$ | oscillator frequency | | 0 | 12 | - | - | MHz |
| $T_{cy(clk)}$ | clock cycle time | see Figure 18 | 83 | - | - | - | ns |
| $f_{CLKLP}$ | low-power select clock frequency | | 0 | 8 | - | - | MHz |
| **Glitch filter** | | | | | | | |
| $t_{gr}$ | glitch rejection time | P1.5/$\overline{RST}$ pin | - | 50 | - | 50 | ns |
| | | any pin except P1.5/$\overline{RST}$ | - | 15 | - | 15 | ns |
| $t_{sa}$ | signal acceptance time | P1.5/$\overline{RST}$ pin | 125 | - | 125 | - | ns |
| | | any pin except P1.5/$\overline{RST}$ | 50 | - | 50 | - | ns |
| **External clock** | | | | | | | |
| $t_{CHCX}$ | clock HIGH time | see Figure 18 | 33 | $T_{cy(clk)} - t_{CLCX}$ | 33 | - | ns |
| $t_{CLCX}$ | clock LOW time | see Figure 18 | 33 | $T_{cy(clk)} - t_{CHCX}$ | 33 | - | ns |
| $t_{CLCH}$ | clock rise time | see Figure 18 | - | 8 | - | 8 | ns |
| $t_{CHCL}$ | clock fall time | see Figure 18 | - | 8 | - | 8 | ns |
| **Shift register (UART mode 0)** | | | | | | | |
| $T_{XLXL}$ | serial port clock cycle time | see Figure 17 | $16T_{cy(clk)}$ | - | 1333 | - | ns |
| $t_{QVXH}$ | output data set-up to clock rising edge time | see Figure 17 | $13T_{cy(clk)}$ | - | 1083 | - | ns |
| $t_{XHQX}$ | output data hold after clock rising edge time | see Figure 17 | - | $T_{cy(clk)} + 20$ | - | 103 | ns |
| $t_{XHDX}$ | input data hold after clock rising edge time | see Figure 17 | - | 0 | - | 0 | ns |
| $t_{XHDV}$ | input data valid to clock rising edge time | see Figure 17 | 150 | - | 150 | - | ns |
| **SPI interface** | | | | | | | |
| $f_{SPI}$ | SPI operating frequency | | | | | | |
| | slave | | 0 | $CCLK/6$ | 0 | 2.0 | MHz |
| | master | | - | $CCLK/4$ | - | 3.0 | MHz |
| $T_{SPICYC}$ | SPI cycle time | see Figure 19, 20, 21, 22 | | | | | |
| | slave | | $6/CCLK$ | - | 500 | - | ns |
| | master | | $4/CCLK$ | - | 333 | - | ns |
| $t_{SPILEAD}$ | SPI enable lead time | see Figure 21, 22 | | | | | |
| | slave | | 250 | - | 250 | - | ns |

**Table 13. Dynamic characteristics (12 MHz)** *...continued*
$V_{DD}$ = 2.4 V to 3.6 V unless otherwise specified.
$T_{amb}$ = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

| Symbol | Parameter | Conditions | Variable clock | | $f_{osc}$ = 12 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{SPILAG}$ | SPI enable lag time | see Figure 21, 22 | | | | | |
| | slave | | 250 | - | 250 | - | ns |
| $t_{SPICLKH}$ | SPICLK HIGH time | see Figure 19, 20, 21, 22 | | | | | |
| | master | | $^2/_{CCLK}$ | - | 165 | - | ns |
| | slave | | $^3/_{CCLK}$ | - | 250 | - | ns |
| $t_{SPICLKL}$ | SPICLK LOW time | see Figure 19, 20, 21, 22 | | | | | |
| | master | | $^2/_{CCLK}$ | - | 165 | - | ns |
| | slave | | $^3/_{CCLK}$ | - | 250 | - | ns |
| $t_{SPIDSU}$ | SPI data set-up time | see Figure 19, 20, 21, 22 | 100 | - | 100 | - | ns |
| | master or slave | | | | | | |
| $t_{SPIDH}$ | SPI data hold time | see Figure 19, 20, 21, 22 | 100 | - | 100 | - | ns |
| | master or slave | | | | | | |
| $t_{SPIA}$ | SPI access time | see Figure 21, 22 | | | | | |
| | slave | | 0 | 120 | 0 | 120 | ns |
| $t_{SPIDIS}$ | SPI disable time | see Figure 21, 22 | | | | | |
| | slave | | 0 | 240 | - | 240 | ns |
| $t_{SPIDV}$ | SPI enable to output data valid time | see Figure 19, 20, 21, 22 | | | | | |
| | slave | | - | 240 | - | 240 | ns |
| | master | | - | 167 | - | 167 | ns |
| $t_{SPIOH}$ | SPI output data hold time | see Figure 19, 20, 21, 22 | 0 | - | 0 | - | ns |
| $t_{SPIR}$ | SPI rise time | see Figure 19, 20, 21, 22 | | | | | |
| | SPI outputs (SPICLK, MOSI, MISO) | | - | 100 | - | 100 | ns |
| | SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$) | | - | 2000 | - | 2000 | ns |
| $t_{SPIF}$ | SPI fall time | see Figure 19, 20, 21, 22 | | | | | |
| | SPI outputs (SPICLK, MOSI, MISO) | | - | 100 | - | 100 | ns |
| | SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$) | | - | 2000 | - | 2000 | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

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**Table 14.　Dynamic characteristics (18 MHz)**

*$V_{DD}$ = 3.0 V to 3.6 V unless otherwise specified.*
*$T_{amb}$ = −40 °C to +85 °C for industrial applications, unless otherwise specified.*[1][2]

| Symbol | Parameter | Conditions | Variable clock | | $f_{osc}$ = 18 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{osc(RC)}$ | internal RC oscillator frequency | | 7.189 | 7.557 | 7.189 | 7.557 | MHz |
| $f_{osc(WD)}$ | internal watchdog oscillator frequency | | 320 | 520 | 320 | 520 | kHz |
| $f_{osc}$ | oscillator frequency | | 0 | 18 | - | - | MHz |
| $T_{cy(clk)}$ | clock cycle time | see Figure 18 | 55 | - | - | - | ns |
| $f_{CLKLP}$ | low-power select clock frequency | | 0 | 8 | - | - | MHz |
| **Glitch filter** | | | | | | | |
| $t_{gr}$ | glitch rejection time | P1.5/$\overline{RST}$ pin | - | 50 | - | 50 | ns |
| | | any pin except P1.5/$\overline{RST}$ | 125 | - | 125 | - | ns |
| $t_{sa}$ | signal acceptance time | P1.5/$\overline{RST}$ pin | - | 15 | - | 15 | ns |
| | | any pin except P1.5/$\overline{RST}$ | 50 | - | 50 | - | ns |
| **External clock** | | | | | | | |
| $t_{CHCX}$ | clock HIGH time | see Figure 18 | 22 | $T_{cy(clk)} - t_{CLCX}$ | 22 | - | ns |
| $t_{CLCX}$ | clock LOW time | see Figure 18 | 22 | $T_{cy(clk)} - t_{CHCX}$ | 22 | - | ns |
| $t_{CLCH}$ | clock rise time | see Figure 18 | - | 5 | - | 5 | ns |
| $t_{CHCL}$ | clock fall time | see Figure 18 | - | 5 | - | 5 | ns |
| **Shift register (UART mode 0)** | | | | | | | |
| $T_{XLXL}$ | serial port clock cycle time | see Figure 17 | $16T_{cy(clk)}$ | - | 888 | - | ns |
| $t_{QVXH}$ | output data set-up to clock rising edge time | see Figure 17 | $13T_{cy(clk)}$ | - | 722 | - | ns |
| $t_{XHQX}$ | output data hold after clock rising edge time | see Figure 17 | - | $T_{cy(clk)} + 20$ | - | 75 | ns |
| $t_{XHDX}$ | input data hold after clock rising edge time | see Figure 17 | - | 0 | - | 0 | ns |
| $t_{XHDV}$ | input data valid to clock rising edge time | see Figure 17 | 150 | - | 150 | - | ns |
| **SPI interface** | | | | | | | |
| $f_{SPI}$ | SPI operating frequency | | | | | | |
| | slave | | 0 | $^{CCLK}/_{6}$ | 0 | 3.0 | MHz |
| | master | | - | $^{CCLK}/_{4}$ | - | 4.5 | MHz |
| $T_{SPICYC}$ | SPI cycle time | see Figure 19, 20, 21, 22 | | | | | |
| | slave | | $^{6}/_{CCLK}$ | - | 333 | - | ns |
| | master | | $^{4}/_{CCLK}$ | - | 222 | - | ns |
| $t_{SPILEAD}$ | SPI enable lead time | see Figure 21, 22 | | | | | |
| | slave | | 250 | - | 250 | - | ns |
| $t_{SPILAG}$ | SPI enable lag time | see Figure 21, 22 | | | | | |
| | slave | | 250 | - | 250 | - | ns |

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**Table 14. Dynamic characteristics (18 MHz)** *…continued*
$V_{DD}$ = 3.0 V to 3.6 V unless otherwise specified.
$T_{amb}$ = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

| Symbol | Parameter | Conditions | Variable clock | | $f_{osc}$ = 18 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | **Min** | **Max** | **Min** | **Max** | |
| $t_{SPICLKH}$ | SPICLK HIGH time | see Figure 19, 20, 21, 22 | | | | | |
| | master | | $^2/_{CCLK}$ | - | 111 | - | ns |
| | slave | | $^3/_{CCLK}$ | - | 167 | - | ns |
| $t_{SPICLKL}$ | SPICLK LOW time | see Figure 19, 20, 21, 22 | | | | | |
| | master | | $^2/_{CCLK}$ | - | 111 | - | ns |
| | slave | | $^3/_{CCLK}$ | - | 167 | - | ns |
| $t_{SPIDSU}$ | SPI data set-up time | see Figure 19, 20, 21, 22 | 100 | - | 100 | - | ns |
| | master or slave | | | | | | |
| $t_{SPIDH}$ | SPI data hold time | see Figure 19, 20, 21, 22 | 100 | - | 100 | - | ns |
| | master or slave | | | | | | |
| $t_{SPIA}$ | SPI access time | see Figure 21, 22 | | | | | |
| | slave | | 0 | 80 | 0 | 80 | ns |
| $t_{SPIDIS}$ | SPI disable time | see Figure 21, 22 | | | | | |
| | slave | | 0 | 160 | - | 160 | ns |
| $t_{SPIDV}$ | SPI enable to output data valid time | see Figure 19, 20, 21, 22 | | | | | |
| | slave | | - | 160 | - | 160 | ns |
| | master | | - | 111 | - | 111 | ns |
| $t_{SPIOH}$ | SPI output data hold time | see Figure 19, 20, 21, 22 | 0 | - | 0 | - | ns |
| $t_{SPIR}$ | SPI rise time | see Figure 19, 20, 21, 22 | | | | | |
| | SPI outputs (SPICLK, MOSI, MISO) | | - | 100 | - | 100 | ns |
| | SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$) | | - | 2000 | - | 2000 | ns |
| $t_{SPIF}$ | SPI fall time | see Figure 19, 20, 21, 22 | | | | | |
| | SPI outputs (SPICLK, MOSI, MISO) | | - | 100 | - | 100 | ns |
| | SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$) | | - | 2000 | - | 2000 | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

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## 10.1 Waveforms

Fig 17. **Shift register mode timing**
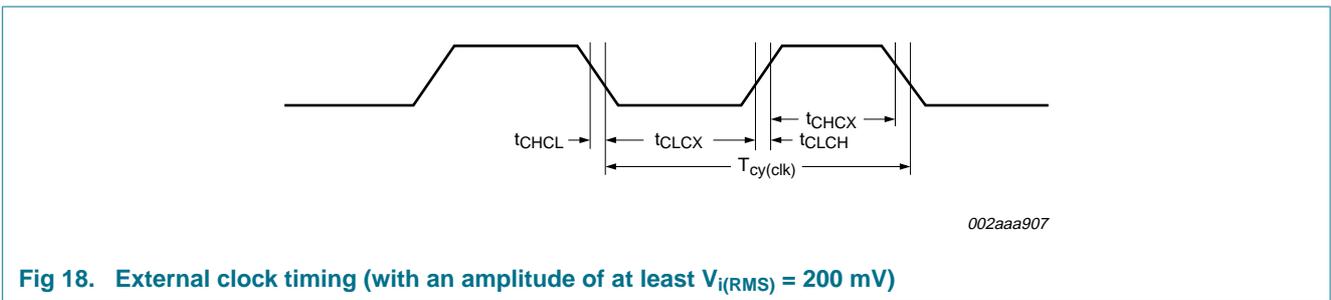
Fig 18. **External clock timing (with an amplitude of at least $V_{i(RMS)} = 200$ mV)**
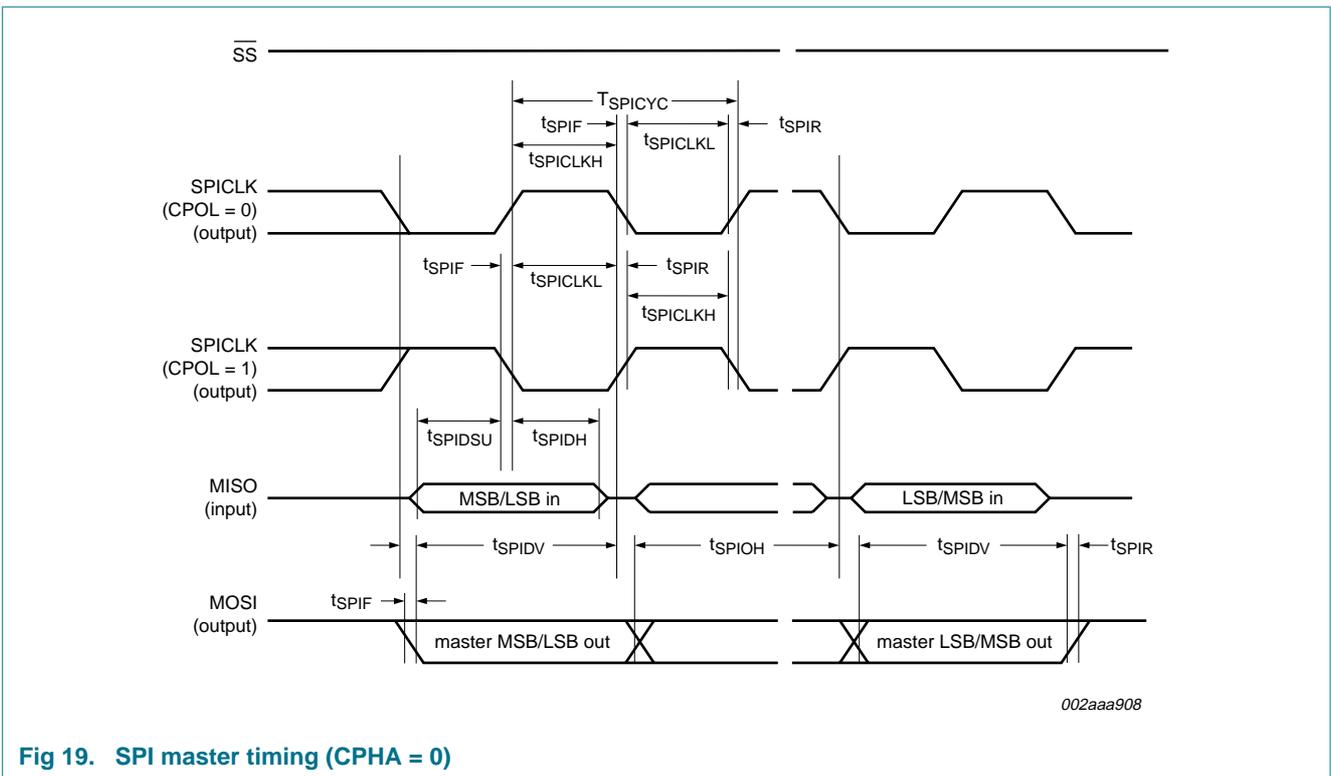
Fig 19. **SPI master timing (CPHA = 0)**

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**Fig 20.  SPI master timing (CPHA = 1)**



**Fig 21.  SPI slave timing (CPHA = 0)**
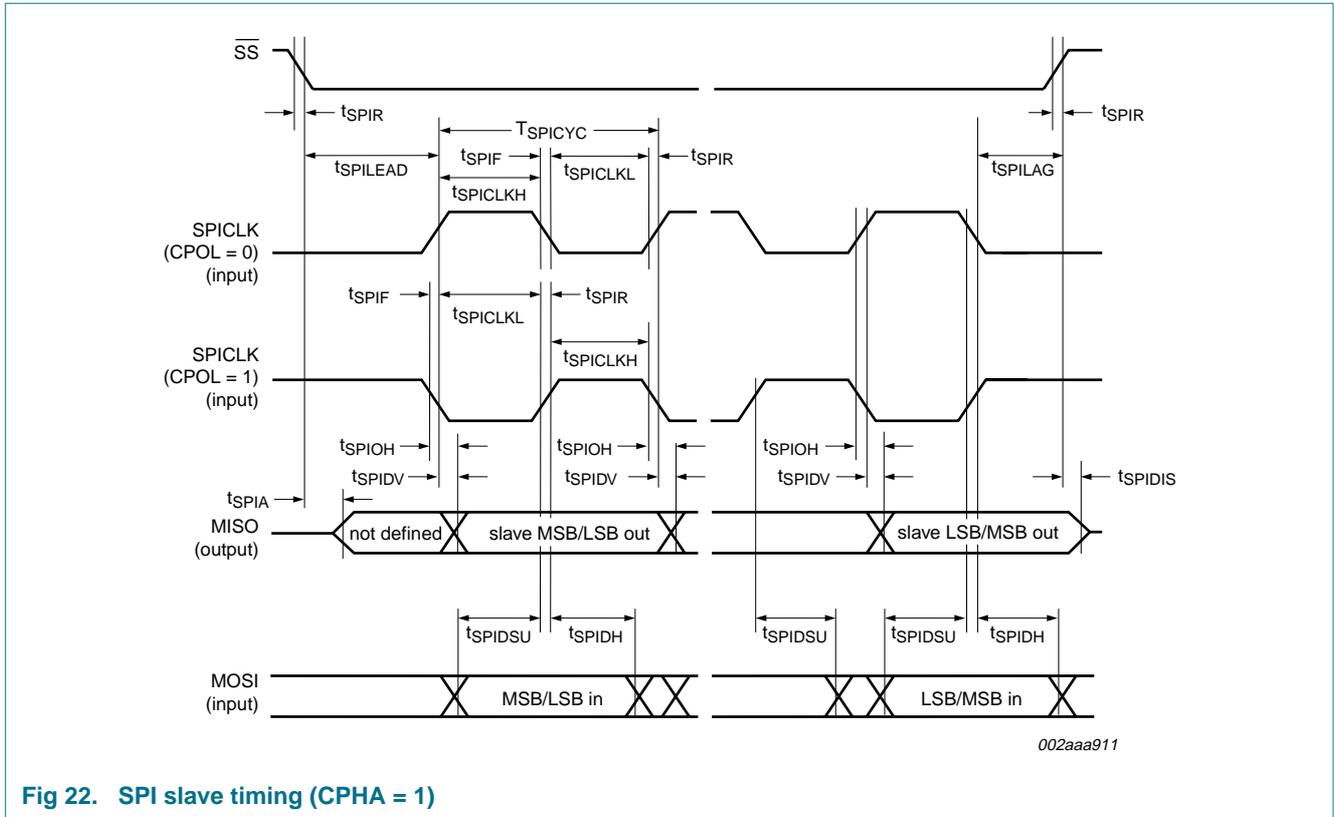
**Fig 22. SPI slave timing (CPHA = 1)**

## 10.2 ISP entry mode

**Table 15. Dynamic characteristics, ISP entry mode**

*$V_{DD}$ = 2.4 V to 3.6 V, unless otherwise specified.*
*$T_{amb}$ = −40 °C to +85 °C for industrial applications, unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $t_{VR}$ | $V_{DD}$ active to $\overline{RST}$ active delay time | | 50 | - | - | μs |
| $t_{RH}$ | $\overline{RST}$ HIGH time | | 1 | - | 32 | μs |
| $t_{RL}$ | $\overline{RST}$ LOW time | | 1 | - | - | μs |
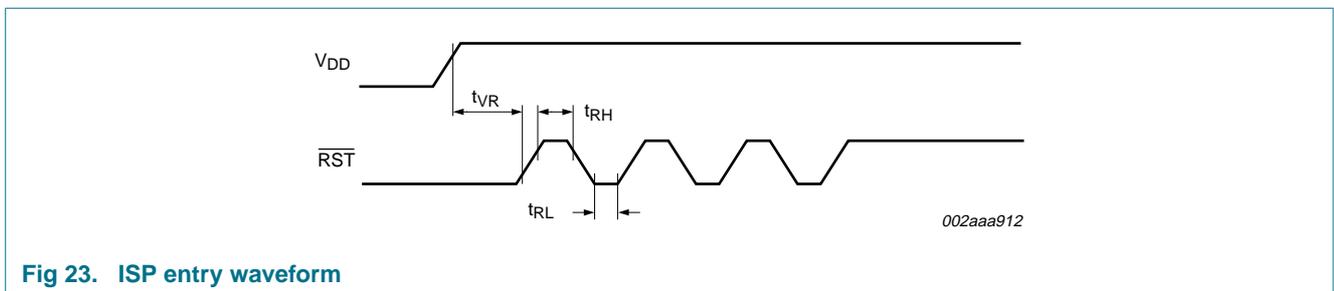


**Fig 23. ISP entry waveform**

# 11. Other characteristics

## 11.1 Comparator electrical characteristics

**Table 16.    Comparator electrical characteristics**
$V_{DD}$ = 2.4 V to 3.6 V, unless otherwise specified.
$T_{amb}$ = −40 °C to +85 °C for industrial applications, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IO}$ | input offset voltage | | - | - | ±20 | mV |
| $V_{IC}$ | common-mode input voltage | | 0 | - | $V_{DD} - 0.3$ | V |
| CMRR | common-mode rejection ratio | [1] | - | - | −50 | dB |
| $t_{res(tot)}$ | total response time | | - | 250 | 500 | ns |
| $t_{(CE-OV)}$ | chip enable to output valid time | | - | - | 10 | µs |
| $I_{LI}$ | input leakage current | $0 V < V_I < V_{DD}$ | - | - | ±10 | µA |

[1]    This parameter is characterized, but not tested in production.

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# 12. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 14 x 14 x 1.4 mm

SOT791-1



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A_1 | A_2 | A_3 | b_p | c | D[1] | E[1] | e | H_D | H_E | L | L_p | v | w | y | Z_D[1] | Z_E[1] | θ |
|------|--------|-----|-----|-----|-----|---|------|------|---|-----|-----|---|-----|---|---|---|--------|--------|---|
| mm | 1.6 | 0.15 0.05 | 1.45 1.35 | 0.25 | 0.45 0.30 | 0.20 0.09 | 14.1 13.9 | 14.1 13.9 | 0.8 | 16.15 15.85 | 16.15 15.85 | 1 | 0.75 0.45 | 0.2 | 0.2 | 0.1 | 1.2 0.8 | 1.2 0.8 | 7° 0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|------|-------|--|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT791-1 | 136E18 | MS-026 | ED-7311EC | | | 02-10-22 |

**Fig 24. Package outline SOT791-1 (LQFP64)**

## 13. Abbreviations

**Table 17.    Acronym list**

| Acronym | Description |
|---------|-------------|
| BOD | Brownout Detect |
| CPU | Central Processing Unit |
| EPROM | Erasable Programmable Read-Only Memory |
| EMI | Electro-Magnetic Interference |
| LCD | Liquid Crystal Display |
| LED | Light Emitting Diode |
| PWM | Pulse Width Modulator |
| RAM | Random Access Memory |
| RC | Resistance-Capacitance |
| RTC | Real-Time Clock |
| SFR | Special Function Register |
| SPI | Serial Peripheral Interface |
| UART | Universal Asynchronous Receiver/Transmitter |
| WDT | WatchDog Timer |

## 14. Revision history

**Table 18.  Revision history**

| Document ID | Release date | Data sheet status | Change notice | Doc. number | Supersedes |
|---|---|---|---|---|---|
| P89LPC9402_1 | 20090422 | Product data sheet | - | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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