NB3N3001

3.3 V 106.25 MHz/ 212.5 MHz PureEdge Clock Generator with LVPECL Differential Output

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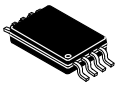
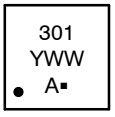


TSSOP−8
DT SUFFIX
CASE 948S

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Description

The NB3N3001 is a low−jitter, dual−rate PLL−synthesized clock generator. It accepts a standard 26.5625 MHz fundamental mode AT cut parallel resonant crystal as the reference source for its integrated crystal oscillator and low noise phase−locked loop (PLL) and produces user selectable clock frequencies of either 106.25 MHz or 212.5 MHz.

In addition, the PLL circuitry will generate a 50% duty cycle square−wave through a pair of differential LVPECL clock outputs. Typical phase jitter at 106.25 MHz is 0.3 ps RMS from 637 kHz to 10 MHz.

The LVPECL output drivers can be disabled to high impedance with the OE pin set LOW. The NB3N3001 operates from a single +3.3 V supply, and is available in both plastic package and die form. The operating temperature range is from −40°C to +85°C.

The NB3N3001 device provides the optimum combination of low cost, flexibility, and high performance which makes it ideal for Fibre−Channel applications.

Features

- PureEdge Clock Family Provides Accuracy and Precision
- Selectable Output Frequency of 106.25 MHz or 212.5 MHz
- Crystal Oscillator Interface Designed for a 26.5625 MHz Crystal
- Fully Integrated Phase−Lock−Loop with Internal Loop Filter
- Differential 3.3 V LVPECL Outputs
- Exceeds Bellcore and ITU Jitter Generation Specification
- RMS Phase Jitter @ 106.25 MHz, using a 26.5625 MHz Crystal (637 kHz − 10 MHz): 0.3 ps (Typical)
- RMS Phase Noise at 106.25 MHz
  Phase Noise:

Offset	Noise Power
100 Hz	−108 dBc/Hz
1 kHz	−122 dBc/Hz
10 kHz	−135 dBc/Hz
100 kHz	−135 dBc/Hz

- Operating Range: V_{CC} = 3.135 V to 3.465 V
- −40°C to +85°C Ambient Operating Temperature
- Small Footprint 8−pin TSSOP Package
- This is a Pb−Free Device

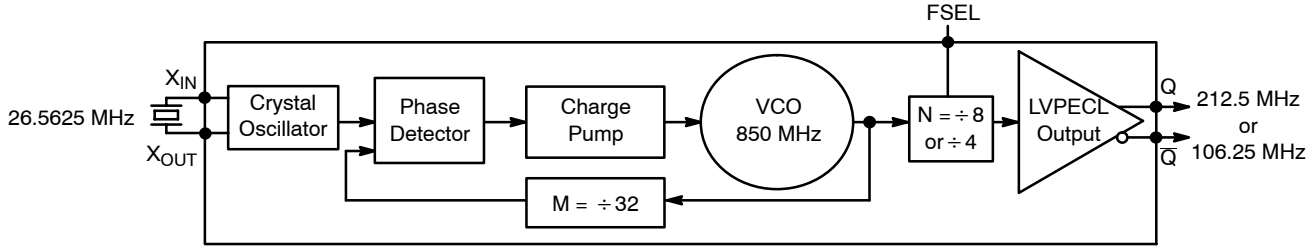


Figure 1. Logic Diagram

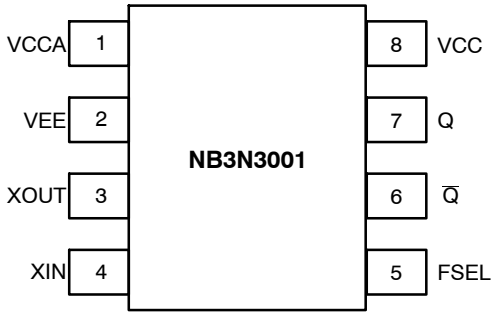


Figure 2. Pinout (Top View)

Table 1. Output Frequency Select

FSEL	Output Frequency (MHz)
0	106.25
1	212.5

NOTE: Input crystal = 26.5625 MHz

Table 2. PIN DESCRIPTION

Pin	Symbol	Type	Description
1	V_{CCA}	Power	Positive analog power supply pin. Connected to V_{CC} with filter components (See Figure 8).
2	V_{EE}	Power	Negative supply pin.
3	X_{OUT}	Input	Crystal input (OUT).
4	X_{IN}	Input	Crystal input (IN).
5	FSEL	LVTTL/LVCMOS Input	Frequency select pin. Defaults LOW when left open. Internal pull down resistor to V_{EE}.
6	$\overline{Q}$	Output	Inverted differential output. Typically terminated with 50 Ω to V_{CC}–2.0 V.
7	Q	Output	Noninverted differential output. Typically terminated with 50 Ω to V_{CC}–2.0 V.
8	V_{CC}	Power	Positive digital core power supply pin. Connected to 3.3 V.

Table 3. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model Machine Model	> 6 kV > 200 V
Moisture Sensitivity (Note 1)	Pb−Free Pkg, TSSOP−8	Level 3
Flammability Rating Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in
Transistor Count		4150
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.6	V
V_I	Inputs		−0.5 to V_{CC} + 0.5	V
I_O	Output Current	Continuous Surge	50 100	mA
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 Lfpm 500 Lfpm	142 103	°C/W
T_{STG}	Storage Temperature		−65 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. POWER SUPPLY DC CHARACTERISTICS, (V_{CC} = 3.3 V ±5%, T_A = −40°C to 85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{CCA}	Analog Supply Current	Included in I_{EE}		19	23	mA
I_{EE}	Power Supply Current			27	31	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. LVPECL DC CHARACTERISTICS, (V_{CC} = 3.3 V ±5%, T_A = −40°C to 85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage (Note 2)		V_{CC} − 1.4		V_{CC} − 0.9	V
V_{OL}	Output Low Voltage (Note 2)		V_{CC} − 2.0		V_{CC} − 1.7	V
V_{SWING}	Peak−to−Peak Output Voltage Swing		0.6	0.75	1.0	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Outputs terminated with 50 Ω to V_{CC} − 2.0 V. See Figures 4 and 12.

Table 7. LVTTL/LVCMOS DC CHARACTERISTICS, (V_{CC} = 3.3 V ±5%, T_A = −40°C to 85°C)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage			2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			−0.3		0.8	V
I_{IH}	Input High Current	FSEL	V_{CC} = V_{IN} = 3.465 V			150	μA
I_{IL}	Input Low Current	FSEL	V_{CC} = 3.465 V, V_{IN} = 0 V	−5.0			μA

Table 8. PIN CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Input Capacitance			4		pF
R_{PD}	Input Pull Down Resistor			100		kΩ

Table 9. CRYSTAL CHARACTERISTICS (Fundamental Mode 18 pF Parallel Resonant Crystal)

Parameter	Conditions	Min	Typ	Max	Unit
Frequency			26.5625		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7.0	pF

Table 10. AC CHARACTERISTICS, (V_{CC} = 3.3 V ±5%, T_A = −40°C to 85°C (Note 4))

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output Frequency	24 MHz – 30 MHz Crystal (Typ. 25 MHz – 26.5625 MHz)		106.25/ 212.5		MHz
$t_{jit(\varnothing)}$	RMS Phase Jitter (Random) (Note 3)	106.25 MHz; Integration Range: 637 kHz –10 MHz		0.3		ps
		212.5 MHz; Integration Range: 637 kHz –10 MHz		0.3		
t_R/t_F	Output Rise/Fall Time	20% to 80% (See Figure 7)	275		600	ps
odc	Output Duty Cycle	(See Figure 6)	48		52	%

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Please refer to the Phase Noise Plot.
4. Output terminated with 50 Ω to V_{CC}– 2.0 V. See Figures 4 and 12.

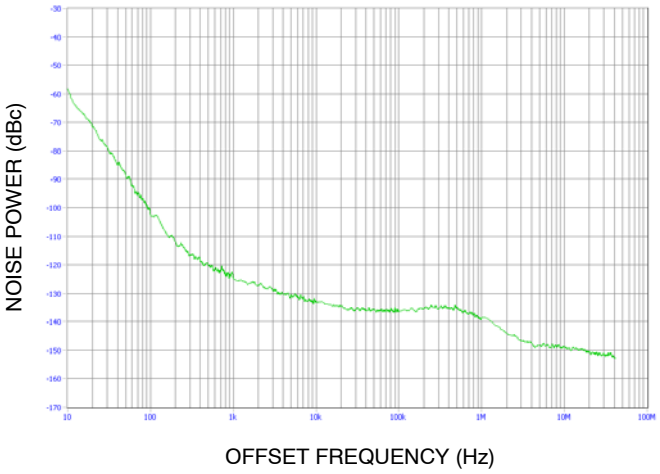


Figure 3. Typical Phase Noise at 106.25 MHz

PARAMETER MEASUREMENT INFORMATION

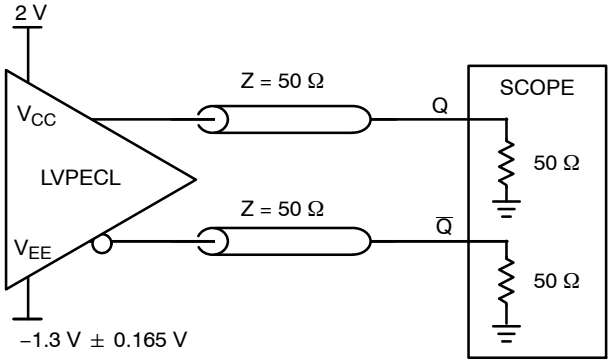


Figure 4. Output Load AC Test Circuit (Split Power Supply)

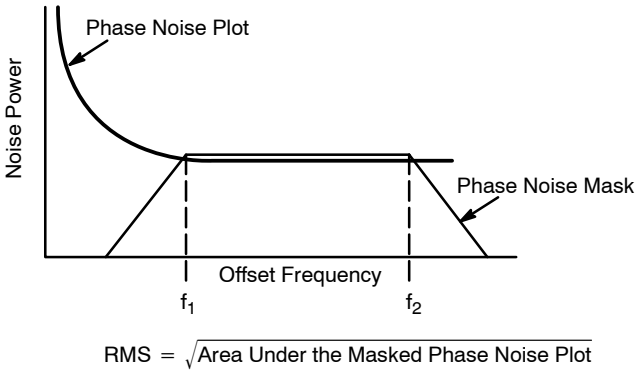


Figure 5. RMS Phase Jitter

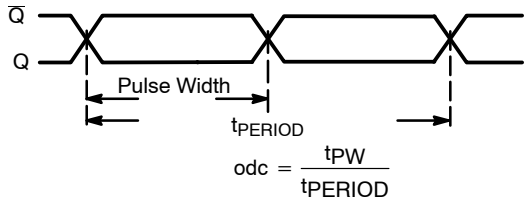


Figure 6. Output Duty Cycle/Pulse Width/Period

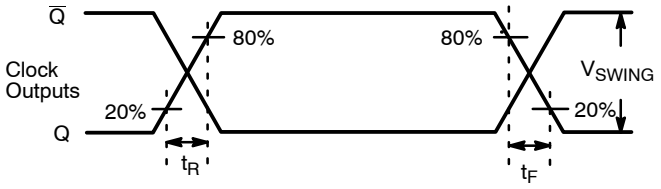


Figure 7. Output Rise/Fall Time

APPLICATION INFORMATION

Power Supply Filtering

The NB3N3001 is a mixed analog/digital product, and as such, it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The NB3N3001 also generates sub−nanosecond output edge rates, and therefore, a good power supply bypassing scheme is a must.

The NB3N3001 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CCA}). The simplest form of noise isolation is a power supply filter on the V_{CCA} pin.

Figure 8 illustrates a typical power supply filter scheme. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

The purpose of this design technique is to try and isolate the high switching noise of the digital outputs from the relatively sensitive internal analog phase−locked loop. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise−related problems in most designs.

Crystal Oscillator Input Interface

The NB3N3001 features an integrated crystal oscillator to minimize system implementation costs. The oscillator circuit is a parallel resonant circuit and thus, for optimum performance, a parallel resonant crystal should be used.

As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the NB3N3001 as possible to avoid any board level parasitics. Surface mount crystals are recommended, but not required.

Figure 9 illustrates a parallel resonant crystal with its associated load capacitors. The capacitor values shown were determined using a 26.5625 MHz, 18 pF parallel resonant crystal and were chosen to minimize the ppm error. Capacitor values can be adjusted slightly for different board layouts to optimize accuracy.

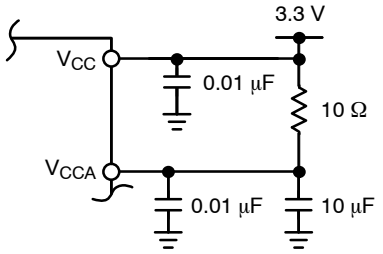


Figure 8. Power Supply Filtering

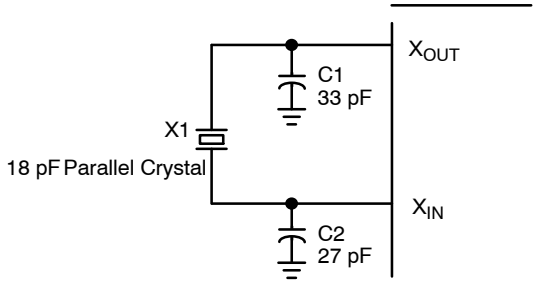


Figure 9. Crystal Input Interface

APPLICATION SCHEMATIC

Figure 10 shows a schematic example of the NB3N3001. An example of LVPECL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the AND8020 Application Note. In this example, an 18 pF parallel resonant 26.5625MHz crystal is used for generating 106.25 MHz output frequency. The C1 = 27 pF and C2 = 33 pF are recommended for frequency accuracy. For different board layout, the C1 and C2 values may be slightly adjusted for optimizing frequency accuracy.

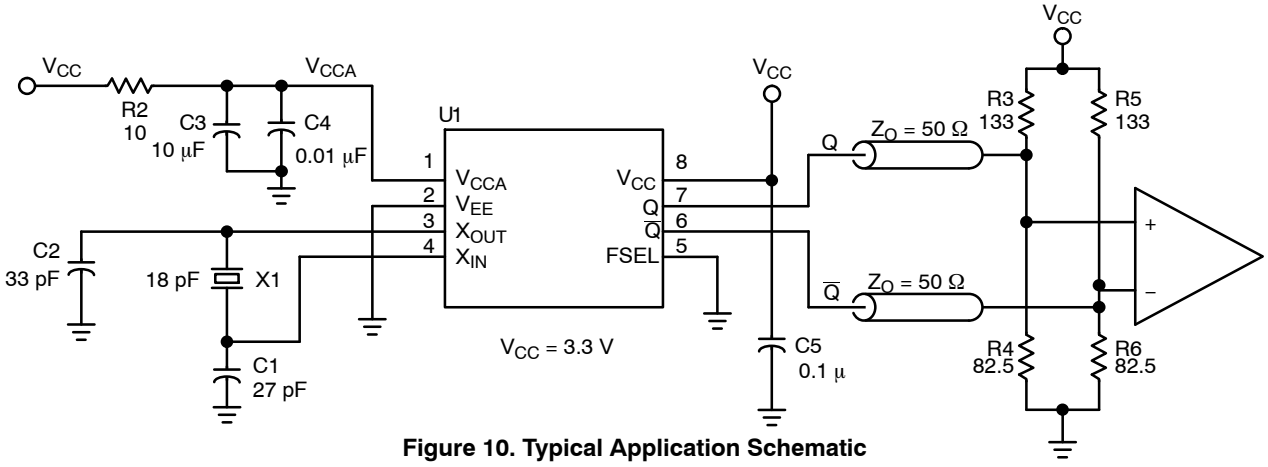


Figure 10. Typical Application Schematic

PC Board Layout Example

Figure 11 shows a representative board layout for the NB3N3001. There exists many different potential board layouts and the one pictured is but one. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through−hole HC49 package. The footprints of other components in this example are listed in Table 11. There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane. The important aspect of the layout in Figure 11 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the NB3N3001 outputs. It is imperative that low inductance chip capacitors are used. It is equally important that the board layout not introduce any of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

The voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device.

Table 11. Footprint Table

Reference	Size
C1, C2	0402
C3	0805
C4, C5	0603
R2	0603

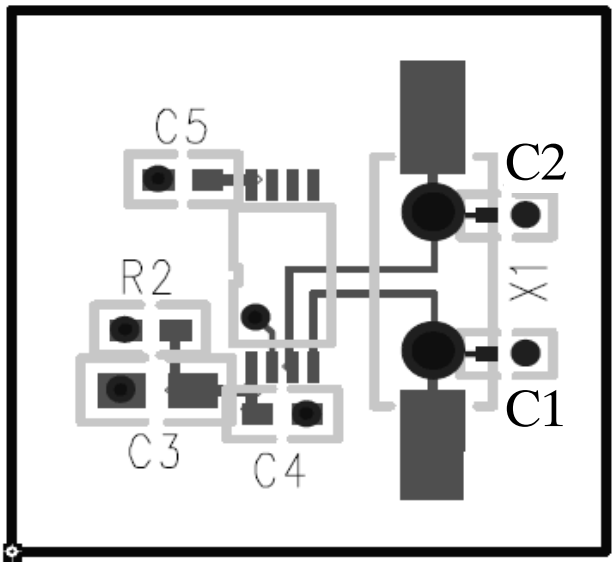


Figure 11. PC Board Layout

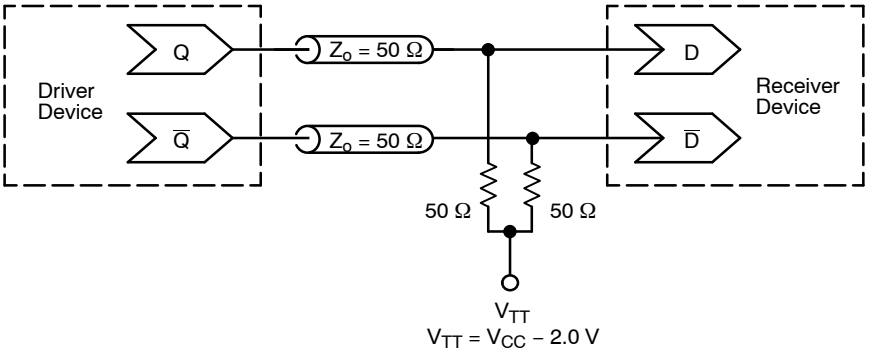


Figure 12. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

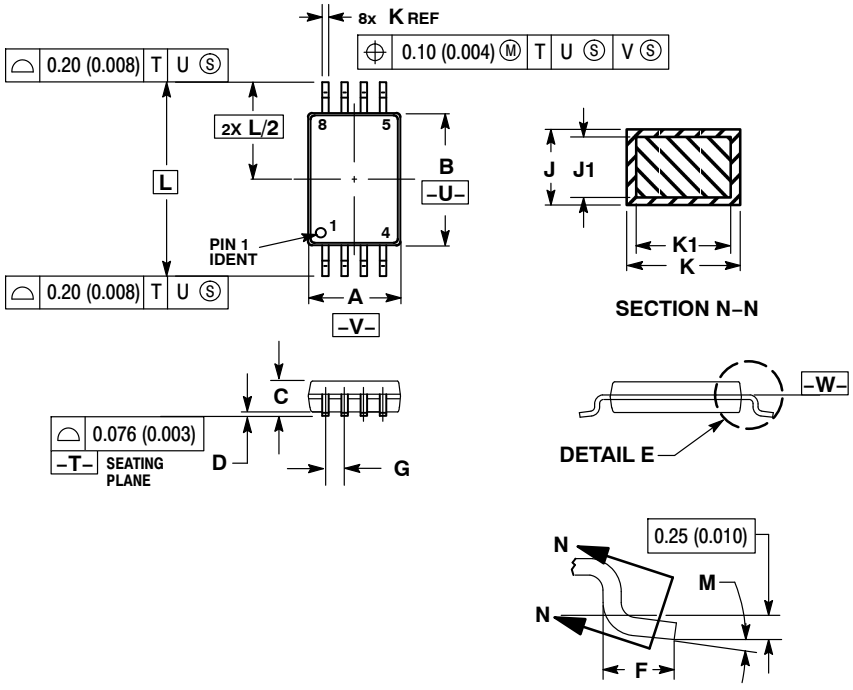
ORDERING INFORMATION

Device	Package	Shipping†
NB3N3001DTG	TSSOP8 4.4 mm (Pb−Free)	100 Units / Rail
NB3N3001DTR2G	TSSOP8 4.4 mm (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

TSSOP−8
CASE 948S−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PUBLICATION ORDERING INFORMATION

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NB3N3001/D