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FAIRCHILD SEMICONDUCTOR

May 1999
Revised October 2006

FSTU32160

16-Bit to 32-Bit Multiplexer/Demultiplexer Bus Switch with −2V Undershoot Protection

General Description

The Fairchild Switch FSTU32160 is a 16-bit to 32-bit high-speed CMOS TTL-compatible multiplexer/demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device can be used in applications where two buses need to be addressed simultaneously. The FSTU32160 is designed so that the A Port demultiplexes into B_1 or B_2 or both. The A and B Ports have "undershoot hardened" circuit protection to support an extended range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit (UHC®) senses undershoot at the I/O's, and responds by preventing voltage differentials from developing and turning on the switch.

Two select (S_1, S_2) inputs provide switch enable control. When S_1, S_2 are HIGH, the device precharges the B Port to a selectable bias voltage (Bias V) to minimize live insertion noise.

Features

- Undershoot hardened to −2V (A and B Ports).
- Slower Output Enable times prevent signal disruption
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.
- See Applications Note AN-5008 for details

Ordering Code:

Order Number	Package Number	Package Description
FSTU32160MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

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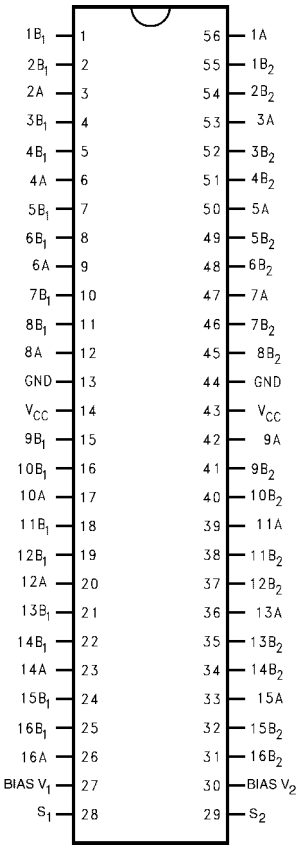
Connection Diagram



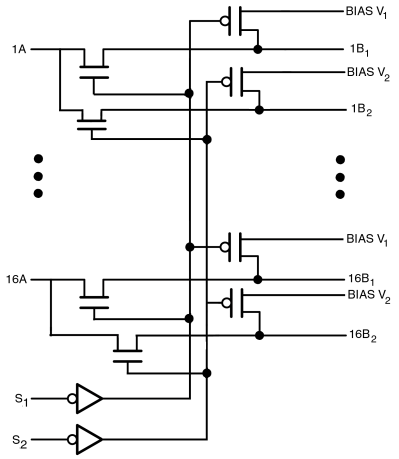
Pin Descriptions

Pin Name	Description
S_1, S_2	Select Inputs
A	Bus A
B_1, B_2	Bus B

Truth Table

Inputs		Function
S_1	S_2	
L	H	x A = x B_1
H	L	x A = x B_2
L	L	x A = x B_1 and x B_2
H	H	x B_1, x B_2 = BiasV

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S) (Note 2)	−2.0V to +7.0V
BiasV Voltage Range	−0.5V to +7.0V
DC Input Control Pin Voltage (V_{IN}) (Note 3)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN} < 0V	−50 mA
DC Output Current (I_{OUT})	128 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100 mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 4)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Precharge Supply (BiasV)	1.5 to V_{CC}
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0 ns/V to 5 ns/V
Switch I/O	0 ns/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: V_S is the voltage observed/applied at either the A or B Ports across the switch.

Note 3: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 4: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 5)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0 ≤ V_{IN} ≤ 5.5V
		0			10	µA	V_{IN} = 5.5V
I_O	Output Current	4.5	0.25			mA	BiasV = 2.4V, S_X = 2.0V B_X = 0
I_{OZH}, I_{OZL}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ A, ≤ V_{CC}, V $BiasV_1$ = $BiasV_2$ = 5.5V
I_{OZH}, I_{OZL}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤ B, ≤ V_{CC}, V $BiasV_1$ = $BiasV_2$ = FLOATING
R_{ON}	Switch On Resistance (Note 6)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64 mA
		4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30 mA
		4.5		8	14	Ω	V_{IN} = 2.4V, I_{IN} = 15 mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15 mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND
I_{BIAS}	Bias Pin Leakage Current	5.5			±1.0	µA	S_1, S_2 = 0V B_X = 0V, $BiasV_X$ = 5.5V
V_{IKU}	Voltage Undershoot	5.5			−2.0	V	0.0 mA ≥ I_{IN} ≥ −50 mA S_1, S_2 = 5.5V

Note 5: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 6: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, RU= RD = 500Ω				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
t_{PHL}, t_{PLH}	A or B, to B or A (Note 7)		0.25		0.25	ns	V_I = OPEN	Figures 2, 3
t_{PZH}	Output Enable Time, S to A, B	7.0	30.0		35.0	ns	V_I = OPEN for t_{PZH} BiasV = GND	Figures 2, 3
t_{PZL}	Output Enable Time, S to A, B	7.0	30.0		35.0	ns	V_I = 7V for t_{PZL} BiasV = 3V	Figures 2, 3
t_{PHZ}	Output Disable Time, S to A, B	1.0	6.9		7.3	ns	V_I = OPEN for t_{PHZ} BiasV = GND	Figures 2, 3
t_{PLZ}	Output Disable Time, S to A, B	1.0	7.7		7.7	ns	V_I = 7V for t_{PLZ}, BiasV = 3V	Figures 2, 3

Note 7: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 8)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	4		pF	V_{CC} = 5.0V
$C_{I/O\ OFF}$	Input/Output Capacitance "OFF State"	8		pF	V_{CC} = 5.0V, Switch OFF

Note 8: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

Undershoot Characteristic (Note 9)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OUTU}	Output Voltage During Undershoot	2.5	$V_{OH} - 0.3$		V	Figure 1

Note 9: This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

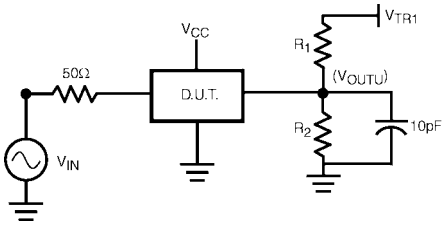
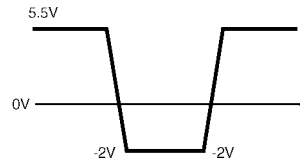


FIGURE 1.

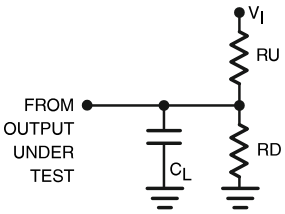
Device Test Conditions

Parameter	Value	Units
V_{IN}	see Waveform	V
$R_1 = R_2$	100K	Ω
V_{TRI}	11.0	V
V_{CC}	5.5	V

Transient Input Voltage (V_{IN}) Waveform



AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω

Note: C_L includes load and stray capacitance, C_L = 50 pF

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 2. AC Test Circuit

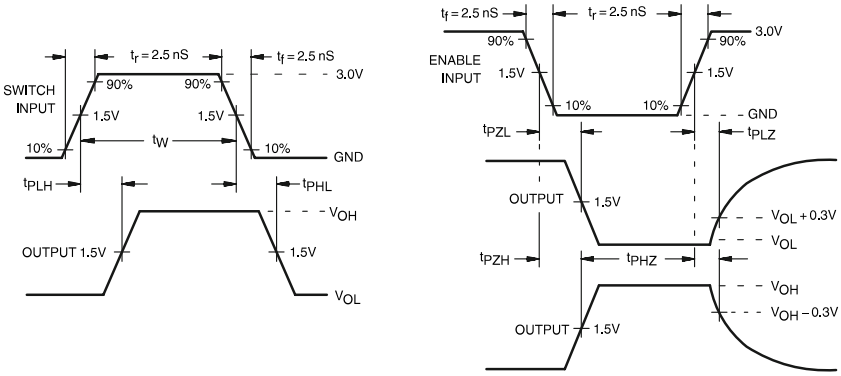
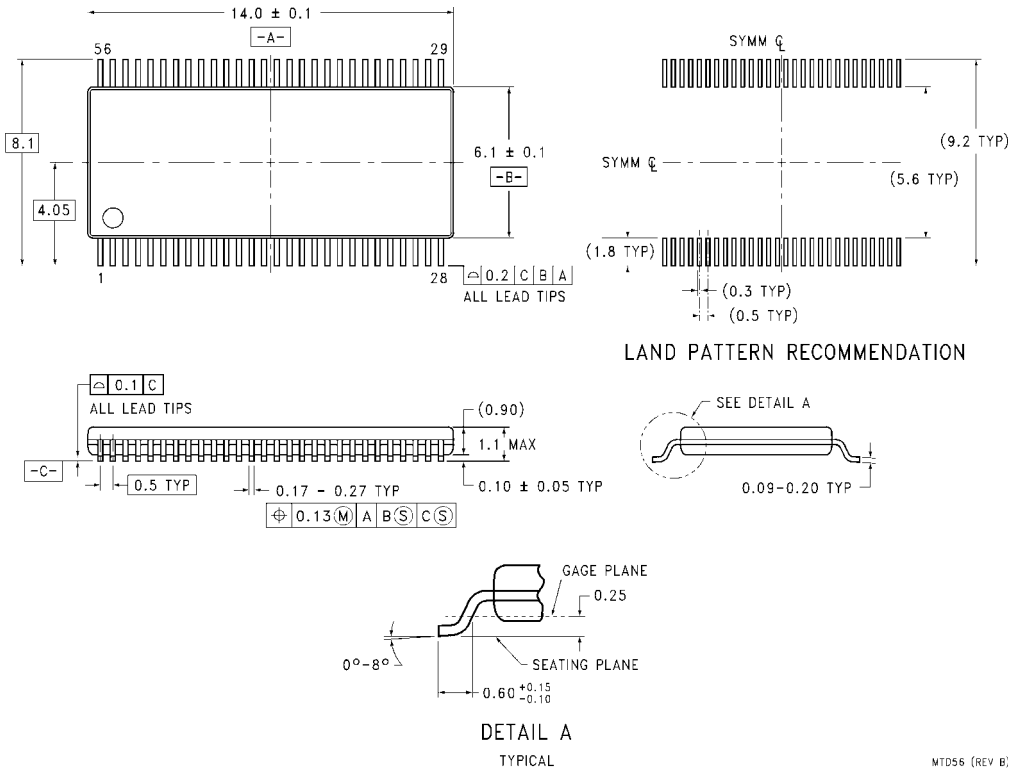


FIGURE 3. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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