PIC18F6310/6410/8310/8410 Rev. C0 Silicon Errata

The PIC18F6310/6410/8310/8410 Rev. C0 parts you have received conform functionally to the Device Data Sheet (DS39635**C**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F6310/6410/8310/8410 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

All of the issues listed here will be addressed in future revisions of the PIC18F6310/6410/8310/8410 silicon.

The following silicon errata apply only to PIC18F6310/6410/8310/8410 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F6310	0000 1011 111	0 0101
PIC18F6410	0000 0110 111	0 0101
PIC18F8310	0000 1011 110	0 0101
PIC18F8410	0000 0110 110	0 0101

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: Master Synchronous Serial Port (MSSP)

Configured in SPI slave mode, the MSSP will generate a write collision if SSPBUF is updated and the previous SSPBUF contents have not been transferred to the shift register.

Reinitializing the MSSP – by clearing and setting the SSPEN bit (SSPCON1<5>) prior to rewriting SSPBUF – will *not* prevent the error condition.

Work around

Prior to updating the SSPBUF register with a new value, verify that the previous contents have been transferred by reading the BF bit (SSPSTAT<0>). If the previous byte has *not* been transferred:

- Update SSPBUF
- If necessary, clear the WCOL bit (SSPCON1<7>)

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: MSSP – Serial Peripheral Interface (SPI)

In SPI mode, the Buffer Full flag (BF bit in the SSPSTAT register), the Write Collision Detect bit (WCOL in SSPCON1) and the Receive Overflow Indicator bit (SSPOV in SSPCON1) are not reset upon disabling the SPI module (by clearing the SSPEN bit in the SSPCON1 register).

For example, if SSPBUF is full (BF bit is set) and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Slave mode, a subsequent write to SSPBUF will result in a write collision. Also, if a new byte is received, a receive overflow will occur.

Work around

If if the buffer is full, before disabling the MSSP module, ensure that:

- SSPBUF is read (thus clearing the BF flag)
- WCOL is clear

If the module is configured in SPI Slave mode, ensure that the SSPOV bit is clear before disabling the module.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: MSSP – I^2C™

In the 10-Bit Slave mode, the I^2C™ mode does not work correctly.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: MSSP – I²C

When configured for I²C™ slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

Work around

The issue can be resolved in either of these ways:

- Prior to the I²C slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPCON2<0>).

- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: MSSP – I²C

The I²C transmission will not work correctly in the MSSP module when it is configured for the I²C Master mode and the device is operating below 3V. The failure can be that the I²C data and clock are not coming out, or a false Acknowledgement will be received, ACKSTAT = 0 (SSPCON2<7>, even if no slave was addressed on the bus.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: Timer1/3

When Timer1 or Timer3 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to `0x0000` when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 1.

EXAMPLE 1: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;          //Stop timer from incrementing
PIE1bits.TMR1IE = 0;           //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                  //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;          //Turn on timer

//Now wait at least two full T1CKI periods + 2TCY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);           //Wait for 2 timer increments more than the Updated Timer
                               //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                         //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;           //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;           //Now re-enable interrupt vectoring for timer 1
```

APPENDIX A: REVISION HISTORY

Rev A Document (12/2008)

First revision of this document. Includes silicon issues 1 (MSSP) 2 (MSSP – SPI) and 3-5 (MSSP – I^2C).

Rev B Document (01/2015)

Added Module 6 (Timer1/3).

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ISBN: 978-1-63276-950-3

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03/25/14