IEEE 802.3 Clause 74 Forward Error Correction v1.0

LogiCORE IP Product Guide

Vivado Design Suite

PG303 (v1.0) April 4, 2018

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Table of Contents

IP Facts

The IEEE 802.3 Clause 74 FEC IP core performs the functions of the IEEE Clause 74 FEC, sometimes known as KR FEC, as described in Clause 74 of IEEE Standard for Ethernet IEEE 802.3-2015.

This core can be used to implement FEC for 10G, 25G, 40G, 50G and 100G Ethernet PHYs, as well as for 16G Fibre Channel (16GFC) links and other standards which use the Clause 74 FEC: see Fibre Channel Framing and Signaling - 4 T11/15-253v2 rev 1.40, INCITS, October 2015, and 25/50G Gigabit Ethernet Consortium Schedule 3 (v1.6).

Features

- The IP core supports encoding and decoding of the (2112,2080) Fire code defined in IEEE Standard for Ethernet IEEE 802.3-2015, Clause 74.

- Suitable for 10GBASE-R, 25GBASE-R, 40GBASE-R, 50GBASE-R, and 100GBASE-R Ethernet PHYs and 16G Fibre Channel PHYs.

- Burst errors of up to 11 bits can be corrected.

- All alignment, transcoding, and scrambling functions are performed within the core.

- Status and control signals allow configuration and statistics monitoring.

- Runtime-configurable error indication bypass mode is available.

- An example design demonstrating the instantiation and use of the IP core is provided.

- The core offers 425 MHz (28 Gb/s) operation in any UltraScale™ or UltraScale+™ device.

IP Facts

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	UltraScale+™, UltraScale™
Supported User Interfaces	Configuration and Status bus

| LogiCORE IP Facts Table	
Resources	Performance and Resource Use web page
Provided with Core	
Design Files	Encrypted RTL
Example Design	Verilog
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	Encrypted Verilog
Supported S/W Driver	N/A
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Design Suite
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado® IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The IEEE 802.3 Clause 74 FEC core implements an encoder and decoder for the (2112,2080) Fire code shortened from the cyclic code of polynomial $x^{32}+x^{23}+x^{21}+x^{11}+x^2+1$, as specified in IEEE Standard for Ethernet IEEE 802.3-2015, Clause 74 for 10GBASE-R PHYs. Burst errors of up to 11 bits can be corrected. Appropriate status and control signals are provided to allow configuration and statistics monitoring as per the IEEE 802.3-2015 MDIO specification for Clause 74.

All UltraScale™ and UltraScale+™ families with suitable transceivers (10 Gb/s or more) are supported. With operating frequencies up to 425 MHz, the core can be used at serial line rates of up to 28 Gb/s. The position of the Clause 74 FEC layer within the Ethernet protocol stack is shown in the following figure.

Figure 1: **Clause 74 FEC Ethernet Layer**
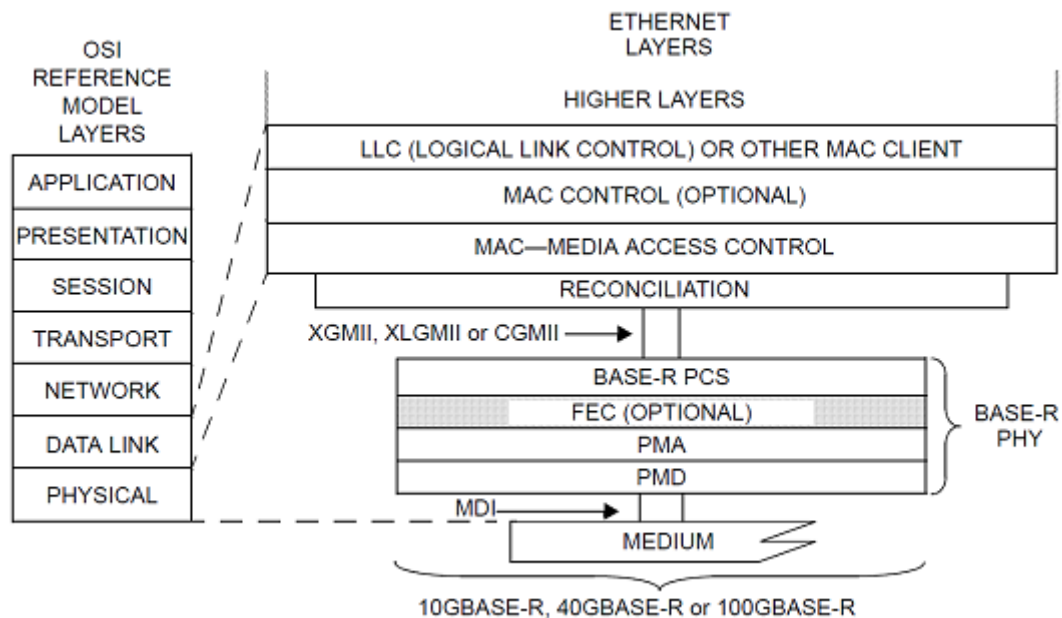
Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado® Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. To generate a full license, visit the product licensing web page. Evaluation licenses and hardware timeout licenses might be available for this core. Contact your local Xilinx sales representative for information about pricing and availability.

Note: To verify that you need a license, check the License column of the IP Catalog. Included means that a license is included with the Vivado® Design Suite; Purchase means that you have to purchase a license to use the core.

For more information about this core, visit the IEEE 802.3 Clause 74 FEC product web page.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

License Checkers

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

Note: IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.

Unsupported Features

The following features of the standard are not supported in the core:

- FEC rapid block synchronization for Energy-Efficient Ethernet (optional feature IEEE Standard for Ethernet IEEE 802.3-2015, Section 74.7.4.8)

Product Specification

Standards

This core adheres to IEEE Standard for Ethernet IEEE 802.3-2015. It is also suitable for use in 16G Fibre Channel systems as described in the Fibre Channel Framing and Signaling - 4 T11/15-253v2 rev 1.40, INCITS, October 2015, Section 5.3.1.

Performance

Latency

The processing latency of the IEEE 802.3 Clause 74 FEC IP core is itemized below. Absolute time values in nanoseconds are given for an operating frequency of 156.25 MHz (10GE operation) and 390.625 MHz (25GE operation). Other operating frequencies can be used and the absolute latency can be obtained by multiplying the latency in clock cycles by the clock period.

Table 1: **Latency**

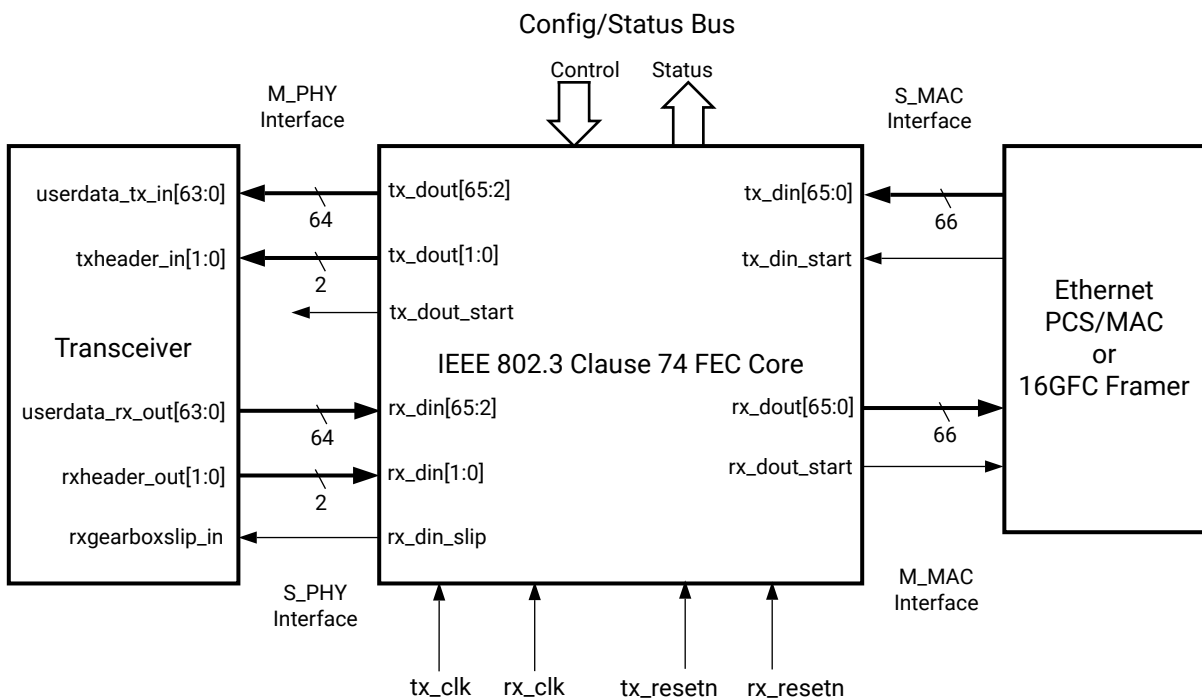| Feature	Latency (cycles)	ns @156.25 MHz	ns @390.625 MHz
Transmit (encode)	5	32.0	12.8
Receive (decode), indication enabled	71	454.4	181.8
Receive (decode), indication bypassed	45	288.0	115.2

Resource Use

For resource use details, visit the Performance and Resource Use web page.

Port Descriptions

The core interfaces are shown in the following figure.

Figure 2: **Core Ports**

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Global Clocks and Resets

Table 2: **Global Clocks and Resets**

Port Name	Direction	Clock	Description
tx_clk	Input		Common TX clock, nominal f_{MAX} 425 MHz
tx_reset	Input	tx_clk	TX reset (active-High)
rx_clk	Input		Common RX clock, nominal f_{MAX} 425 MHz
rx_reset	Input	rx_clk	RX reset (active-High)

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Transmit Interface

Table 3: **Transmit Interface**

Port Name	Direction	Clock	Description
tx_din_start	Input	tx_clk	Indicates first cycle of input codeword to encoder
tx_din[65:0]	Input	tx_clk	66-bit input data. Sync header in [1:0], payload in [65:2]. Bit 0 is input first.
tx_dout_start	Output	tx_clk	Indicates first cycle of output codeword from encoder
tx_dout[65:0]	Output	tx_clk	66-bit FEC-encoded output data. Bit 0 is transmitted first.

The IEEE 802.3 Clause 74 FEC encoder accepts a 66-bit data stream in standard 64b/66b encoding. It transcodes this data to compress the 2-bit synchronization headers, appends parity bits, and finally scrambles the codeword to produce a 66-bit stream according to the FEC algorithm of IEEE Standard for Ethernet IEEE 802.3-2015, Clause 74.7.4.

Receive Interface

The IEEE 802.3 Clause 74 FEC decoder accepts a 66-bit data stream containing FEC-encoded data. It performs alignment as described in IEEE Standard for Ethernet IEEE 802.3-2015, Clause 74.7.4.5.1 by searching the incoming data for codewords which can be successfully decoded, making use of the transceiver gearbox slip function. It then extracts the parity words and decodes the received data, correcting burst errors of up to 11 bits in length. Status flags are pulsed once per output codeword to indicate the decoding status of each block. Finally, the corrected data is de-transcoded to restore the 64b/66b sync headers which were compressed during transcoding.

When error indication is disabled (`ctrl_rx_indication_en` set to 0), the decoder passes out the received data of an uncorrectable codeword on `rx_dout[65:0]` as it was received, without indicating that it might contain erroneous bits.

When error indication is enabled (`ctrl_rx_indication_en` set to 1), the 32 66-bit output words corresponding to an uncorrectable codeword have their sync headers set to binary 11 (invalid) to indicate that the data is unreliable.

Sync header error marking is performed according to the pattern in `ctrl_rx_header_mark[31:0]`. If bit 0 of this vector is set to 1, the sync header of the first block is set to 11. If bit 1 is set to 1, the second sync header is set to 11, and so on up to bit 31 which controls the erroring of the final sync header of the codeword. This feature allows the IEEE 802.3 Clause 74 FEC IP core to be used in 10GBASE-R, 25GBASE-R, 40GBASE-R, 50GBASE-R, and 100GBASE-R PHYs, or custom systems where a different pattern of sync header corruption is required for uncorrectable codewords.

If either of the `ctrl_rx_indication_en` and `ctrl_rx_header_mark[31:0]` signals is changed while the core is operating, the changes take effect instantly; the signals are not sampled at reset. In the case of `ctrl_rx_indication_en`, this causes a jump in the decoded output stream because the receiver latency differs between indication enabled mode and indication bypass mode. The IEEE 802.3 Clause 74 FEC IP core remains synchronized to the incoming data when switching modes.

The `ctrl_rx_indication_en` and `ctrl_rx_header_mark[31:0]` signals can be tied to all-zero if not required.

Table 4: **Receive Interface**

Port Name	Direction	Clock	Description
rx_din_slip	Output	rx_clk	Requests the transceiver receive gearbox to perform a bit slip
rx_din[65:0]	Input	rx_clk	66-bit input data from the transceiver. Bit 0 is received first.
rx_dout_start	Output	rx_clk	Indicates first cycle of output codeword from decoder
rx_dout[65:0]	Output	rx_clk	66-bit corrected data from decoder. Sync header in [1:0], payload in [65:2]. Bit 0 transmitted first.
ctrl_rx_header_mark[31:0]	Input	rx_clk	Controls header marking when error indication is enabled.
ctrl_rx_indication_en	Input	rx_clk	Controls whether error indication is enabled or disabled in the receiver.
stat_rx_aligned	Output	rx_clk	A value of 1 indicates that the receiver has successfully aligned to the data stream. 0 indicates lack of alignment.
stat_cw_uncorrected	Output	rx_clk	Pulsed for one cycle when an uncorrected codeword was processed
stat_cw_corrected	Output	rx_clk	Pulsed for one cycle when a corrected codeword was processed
stat_cw_inc	Output	rx_clk	Pulsed for one cycle when any codeword was processed

Designing with the Core

Clocking

The IEEE 802.3 Clause 74 FEC core has two clock inputs. The clocks are `tx_clk` (transmit) and `rx_clk` (receive).

Transmit Clock

This clock must be provided to both the core and serial transceiver. Serial signaling rates up to 28.05 GBd are supported, and this clock therefore has a nominal maximum frequency of 425 MHz. The typical clock rate for 25G Ethernet operation is 390.625 MHz. For 10G Ethernet, 156.25 MHz should be used.

Receive Clock

This clock is typically provided by the serial transceiver (GT) to clock the FEC receiver logic so that the required throughput is maintained throughout the receive path. The nominal clock rates are the same as for the transmit clock.

Resets

The core has two resets, one per clock domain. They are `tx_resetn` (transmit) and `rx_resetn` (receive). All resets are active-Low.

During configuration, the resets must be asserted Low. When the clocks are stable, the resets must be released. The resets can be asserted and deasserted independently; resetting the receive path has no effect on the transmit path, and similarly resetting the transmit path has no effect on the receive path. The reset procedure is simple and the only requirement is that a reset must be asserted until the corresponding clock(s) are stable.

Protocol Description

Transmit Operation

The following figure shows the timing of data transfers through the transmit path of the IEEE 802.3 Clause 74 FEC core.

Figure 3: **Data Transfer Timing through the Transmit Path**
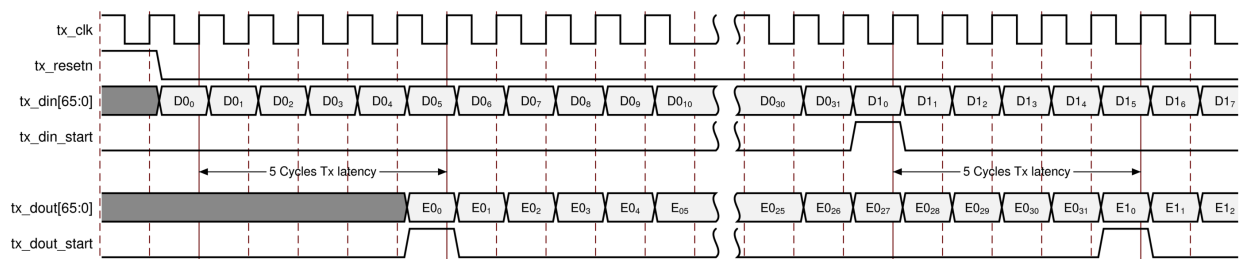

All Clause 74 FEC codewords are 2112 bits long, and therefore take 32 clock cycles to transfer across the 66-bit interfaces of the core. Within each data word, bit 0 (the least significant bit) is considered to be the first bit transmitted in time.

The use of the `tx_din_start` port is optional. It can be pulsed to indicate that the current data word on `tx_din` is to become the first 66-bit block within a new FEC codeword. If control of the location of the codeword boundaries within the transmitted data stream is required, this input must be pulsed at the start of each codeword as shown on the right-hand side of the figure above. If this port is not used (tied Low), the core starts processing codewords at an arbitrary point within the incoming data stream. If `tx_din_start` is driven High mid-way through a codeword, the core abandons the current encoding operation and begins processing a new codeword starting at the requested location.

Receive Operation

The following figure shows the alignment procedure for the core.

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Figure 4: **Alignment Procedure**
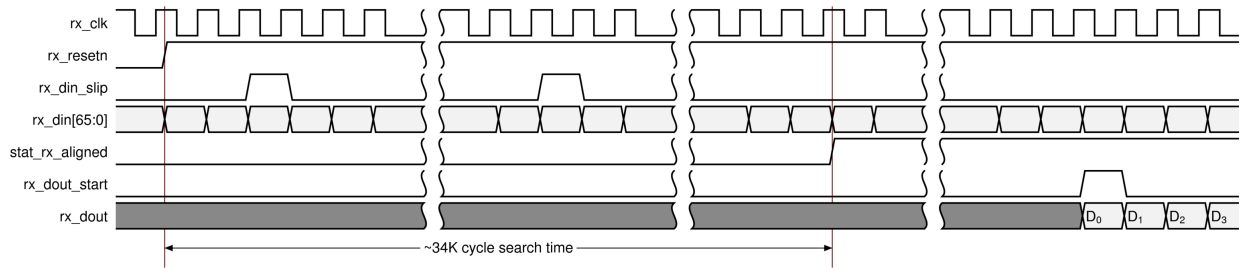
Synchronization is performed according to Section 74.7.4.7 of IEEE Standard for Ethernet IEEE 802.3-2015. For the synchronization procedure to operate correctly, the `rx_din_slip` port must be connected to the receiver gearbox slip control of the transceiver that is receiving the Clause 74-encoded data stream. The FEC alignment logic asserts this signal periodically during the alignment process to request that the deserializer drop a bit from the data stream. This allows all possible start positions in the data stream to be tested.

The alignment procedure can take an extended period of time (up to 68,000 clock cycles in the absence of errors in the input data). When alignment is found, the core drives `stat_rx_aligned` High and begins outputting decoded data on the `rx_dout` port.

Note: The optional FEC rapid block synchronization for the Energy-Efficient Ethernet feature described in IEEE Standard for Ethernet IEEE 802.3-2015, Section 74.7.4.8 is not supported by this core.

The figure below shows the timing of the data and statistics interface of the FEC receive interface. In the transmit interface, each codeword lasts 32 clock cycles and the bit ordering is considered to be least significant bit first.

Figure 5: **Data and Statistics Interface Timing (FEC Receive Interface)**
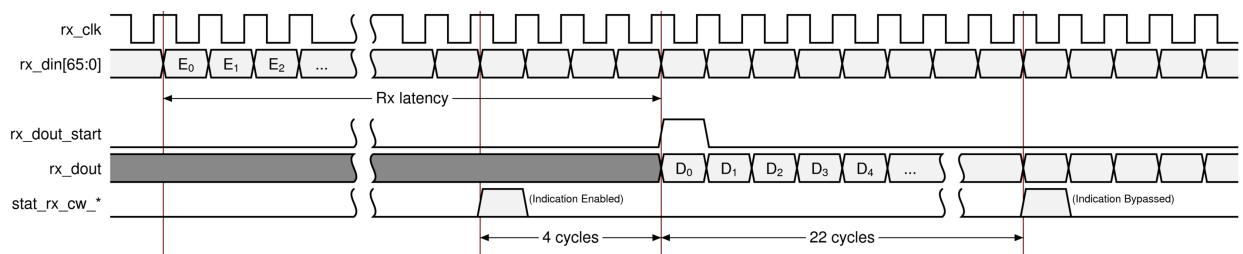
The receive datapath latency depends on the setting of `ctrl_rx_indication_en`. When this control is driven High, the indication of uncorrectable errors (by marking 66b headers with a 11 pattern) is enabled and the latency of the decoder is increased. In this mode, the codeword statistics flags are driven four cycles in advance of the start of the corresponding codeword output.

When `ctrl_rx_indication_en` is Low, error indication is disabled and the latency of the decoder is reduced. In this mode, the codeword statistics flags are driven 22 cycles after the start of the corresponding codeword output.

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Design Flow Steps

This section describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)

- *Vivado Design Suite User Guide: Designing with IP* (UG896)

- *Vivado Design Suite User Guide: Getting Started* (UG910)

- *Vivado Design Suite User Guide: Logic Simulation* (UG900)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado® Design Suite.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.

2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) and the *Vivado Design Suite User Guide: Getting Started* (UG910).

Figures in this chapter are illustrations of the Vivado IDE. The layout depicted here might vary from the current version.

User Parameters

There are no user-configurable parameters.

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Core Configuration

When installed, the IEEE 802.3 Clause 74 FEC IP core appears in the Vivado® IP catalog under the category Communication & Networking, sub-category Error Correction. The IEEE 802.3 Clause 74 FEC IP core has no user configuration parameters or optional ports. An example screenshot of the IEEE 802.3 Clause 74 FEC IP core customization screen is shown below.

Figure 6: **Core Customization Screen**
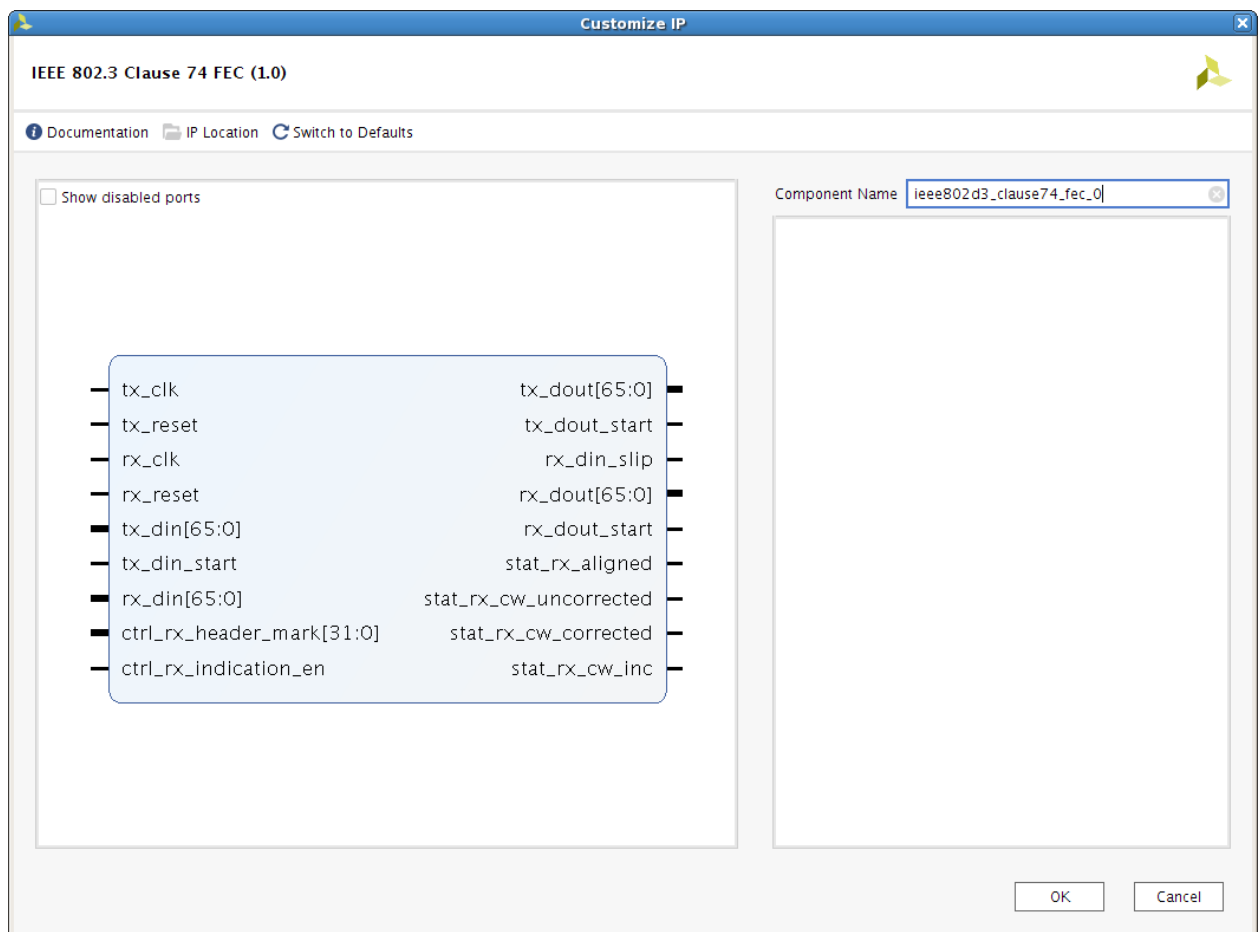
Constraining the Core

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

For comprehensive information about Vivado® simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900).
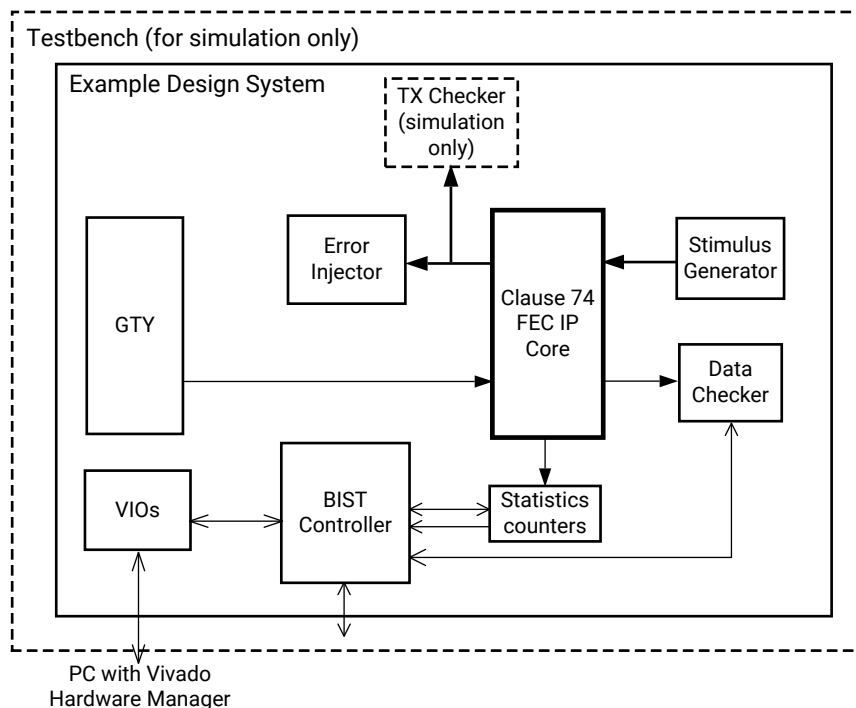
Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Example Design

The IEEE 802.3 Clause 74 FEC IP core includes an example design demonstrating the connectivity and use of the IP. To generate the example design, first create an instance of the IP in any Vivado® project. Then right-click on the instance within the Sources panel and choose **Open IP Example Design...** from the context menu. You can choose the directory in which the example design is created.

The example design includes a fully synthesizable self-checking test harness for the IEEE 802.3 Clause 74 FEC IP core which demonstrates all the major features of the core. In simulation it runs a set of tests which include the correction of correctable errors, the detection of uncorrectable errors, and the verification of the alignment process. Encoded data is compared against a behavioral model of the Clause 74 encode function to establish correctness relative to the standard. A block diagram of the example design is shown below.

Figure 7: **Example Design**

Testbench (for simulation only)

Example Design System

TX Checker (simulation only)

Error Injector

Stimulus Generator

GTY

Clause 74 FEC IP Core

Data Checker

VIOs

BIST Controller

Statistics counters

PC with Vivado Hardware Manager

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The example design can be generated for implementation on any compatible Xilinx® device or development board. If the chosen board is a VCU108 or VCU118 development platform, pinout constraints are automatically included to enable bitstream generation and download. For other platforms, you must consult the product guide and enter appropriate pinout constraints for your system.

The example design relies on the presence of a free-running 300 MHz input clock as well as a 156.25 MHz GT reference clock.

When synthesized and implemented in hardware, the example design can be used to perform automatic testing (BIST) and also manual testing of the IEEE 802.3 Clause 74 FEC IP core. The BIST functionality is similar to the testing that is performed in simulation but more extensive, running many hundreds of thousands of codewords through the encoder and decoder.

Control and monitoring of the example design is achieved using a pair of VIO cores embedded in the design. An example of a Vivado® Hardware Manager configuration screen for control and monitoring is shown in the figure below.

Figure 8: **Vivado Hardware Manager**

Example Design Port Names

The available signals on these VIOs and their functions are described in the following table.

Table 5: **Example Design Port Names**

Port name	Direction	VIO	Description
stat_bist_pass	Input	hw_vio_2	Indicates built-in self-test sequence has passed.
stat_bist_fail	Input	hw_vio_2	Indicates built-in self-test sequence has failed.
stat_bist_running	Input	hw_vio_2	Indicates built-in self-test sequence is running.
stat_bist_code[7:0]	Input	hw_vio_2	Indicates error code from BIST. For successful BIST the code always reads as 0x00.
ctrl_bist_start_vio	Output	hw_vio_2	Pulsing this signal High causes the BIST sequence to start.
ctrl_indication_enable	Output	hw_vio_2	This signal directly controls the ctrl_rx_indication_en core input, described above.
inj_uncorr_vio	Output	hw_vio_1	Pulsing this signal High causes an uncorrectable error to be injected into the FEC encoded data stream.
inj_corr_vio	Output	hw_vio_1	Pulsing this signal High causes a correctable error to be injected into the FEC encoded data stream.
inj_slip_vio	Output	hw_vio_1	Pulsing this signal High causes the transceiver gearbox to slip. This can be used to test that the core loses and regains alignment when the data stream is interrupted.
rx_total_vio[31:0]	Input	hw_vio_1	This 32-bit counter records the total number of codewords processed by the FEC decoder.
rx_noerrors_vio[31:0]	Input	hw_vio_1	This 32-bit counter records the number of codewords processed by the FEC decoder which contained no errors.
rx_corrected_vio[31:0]	Input	hw_vio_1	This 32-bit counter records the total number of codewords processed by the FEC decoder which contained correctable errors.
rx_uncorrected_vio[31:0]	Input	hw_vio_1	This 32-bit counter records the total number of codewords processed by the FEC decoder which contained uncorrectable errors.
rx_data_fails_vio[31:0]	Input	hw_vio_1	This 32-bit counter records the total number of times the built-in data checker saw an unexpected mismatch.
rx_unlocks_vio[31:0]	Input	hw_vio_1	This 32-bit counter records the total number of times the FEC receiver alignment status was seen to transition from High to Low, indicating loss of alignment.
reset_statistics_vio	Output	hw_vio_1	Pulsing this signal High resets all the 32-bit statistics counters described above.
stat_rx_align_status_vio	Input	hw_vio_2	This signal reflects the status of the stat_rx_aligned output from the core.
stat_checker_locked_vio	Input	hw_vio_2	This signal is High when the built-in data checker has locked to the decoded output data from the FEC.

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Table 5: **Example Design Port Names** *(cont'd)*

Port name	Direction	VIO	Description
stat_phy_gt_reset_rx_done_vio	Input	hw_vio_2	This signal indicates that the transceiver RX-side reset sequence has completed successfully.
stat_phy_gt_reset_tx_done_vio	Input	hw_vio_2	This signal indicates that the transceiver TX-side reset sequence has completed successfully.
phy_loopback	Output	hw_vio_2	This signal should be set to 1 to enable loopback within the transceiver. It can only be set to 0 if a physical external loopback is present on the board.
vio_reset	Output	hw_vio_1	Driving this signal High puts the example design into a reset state. Driving this signal Low releases the global reset.

Upgrading

This appendix is not applicable for the first release of the core.

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Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

Note: IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.

Finding Help on Xilinx.com

To help in the design and debug process when using the core, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the core. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx® Documentation Navigator. Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the Core

AR 70776.

Technical Support

Xilinx provides technical support in the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Debug Tools

There are many tools available to address IEEE 802.3 Clause 74 FEC design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx® devices.

The Vivado logic analyzer is used to interact with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908).

Hardware Debug

Hardware issues can range from link bring-up to problems seen after hours of testing. This section provides debug steps for common issues. The Vivado® debug feature is a valuable resource to use in hardware debug. The signal names mentioned in the following individual sections can be probed using the debug feature for debugging the specific problems.

General Checks

Ensure that all the timing constraints for the core were properly incorporated from the example design and that all constraints were met during implementation.

- Does it work in post-place and route timing simulation? If problems are seen in hardware but not in timing simulation, this could indicate a PCB issue. Ensure that all clock sources are active and clean.
- If using MMCMs in the design, ensure that all MMCMs have obtained lock by monitoring the locked port.
- If your outputs go to 0, check your licensing.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help→Documentation and Tutorials**.
- On Windows, select **Start→All Programs→Xilinx Design Tools→DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this product guide:

1. IEEE Standard for Ethernet IEEE 802.3-2015
2. Fibre Channel Framing and Signaling - 4 T11/15-253v2 rev 1.40, INCITS, October 2015
3. 25/50G Gigabit Ethernet Consortium Schedule 3 (v1.6)
4. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
5. *Vivado Design Suite User Guide: Designing with IP* (UG896)
6. *Vivado Design Suite User Guide: Getting Started* (UG910)
7. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
8. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)

Training Resources

1. Vivado Design Suite Hands-on Introductory Workshop
2. Vivado Design Suite Tool Flow

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
04/04/2018	
Initial Xilinx release.	

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