PSMNR90-30BL

N-channel 30 V 1.0 mΩ logic level MOSFET in D2PAK

2 April 2014 **Product data sheet**

1. General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

3. Applications

- DC-to-DC converters
- Load switiching
- Motor control
- Server power supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 175 °C		-	-	30	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; Fig. 2	[1]	-	-	120	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	306	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	0.89	1	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; Fig. 13; Fig. 12		-	1.19	1.5	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V_{GS} = 4.5 V; I_D = 75 A; V_{DS} = 15 V; Fig. 14; Fig. 15		-	37	-	nC
$Q_{G(tot)}$	total gate charge			-	118	-	nC

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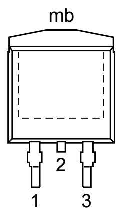
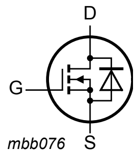
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 120 A; V_{sup} ≤ 30 V; R_{GS} = 50 Ω; unclamped		-	-	1.9	J

[1] Continuous current is limited by package.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 **D2PAK (SOT404)**	
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR90-30BL	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR90-30BL	PSMNR90-30BL

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 175 °C		-	30	V
V_{DGR}	drain-gate voltage	T_j ≥ 25 °C; T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	30	V

Symbol	Parameter	Conditions		Min	Max	Unit
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	306	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2	[1]	-	120	A
		V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	120	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	1573	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	120	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1573	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 120 A; V_{sup} ≤ 30 V; R_{GS} = 50 Ω; unclamped		-	1.9	J

[1] Continuous current is limited by package.

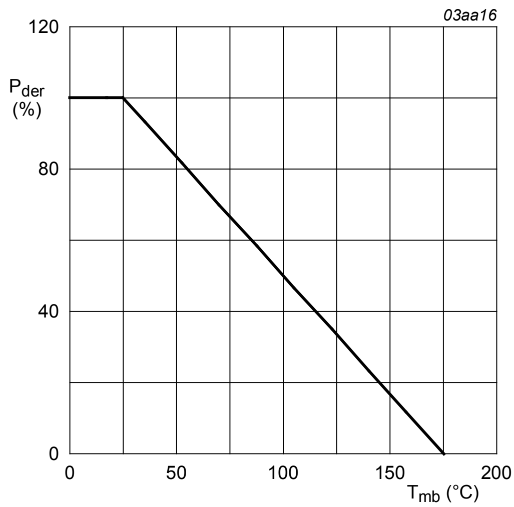


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

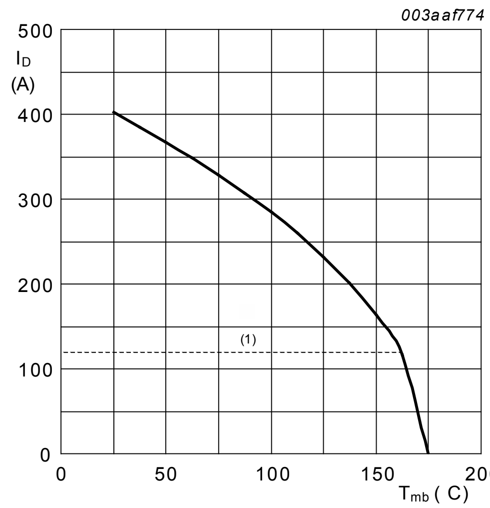


Fig. 2. Continuous drain current as a function of mounting base temperature.

$V_{GS} \geq 10$ V; (1) Capped at 120 A due to package

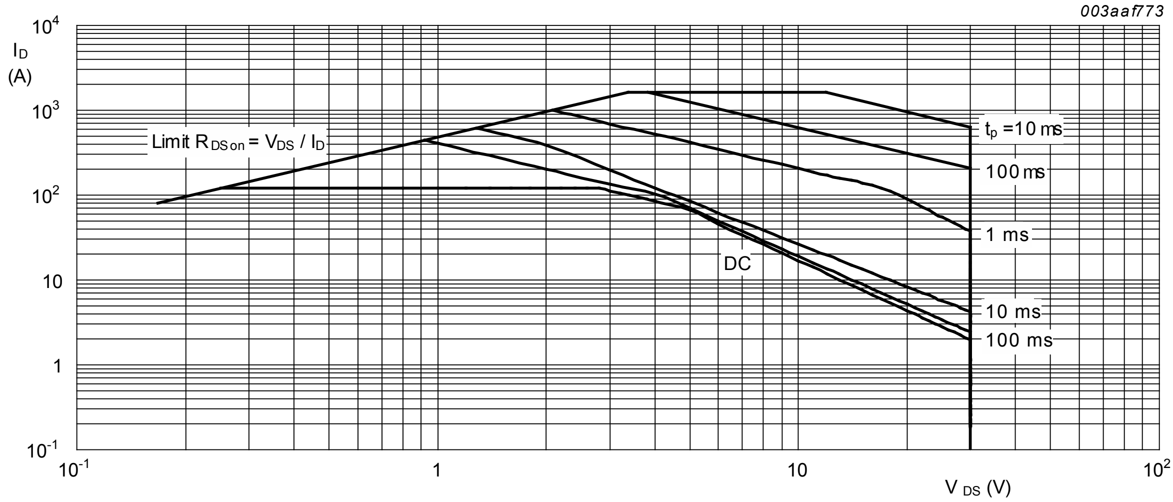


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

T_{mb} = 25 °C; I_{DM} is a single pulse; Capped at 120 A due to package

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	0.22	0.49	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board		-	50	-	K/W

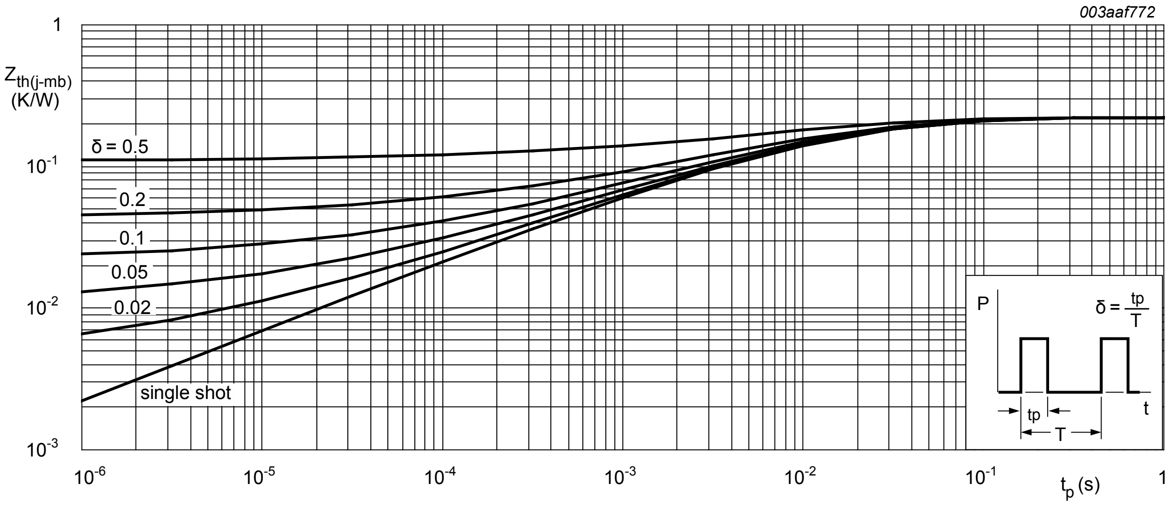


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		30	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 10; Fig. 11		1.3	1.7	2.2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 11		0.65	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 11		-	-	2.5	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C		-	0.02	10	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	0.89	1	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	1.1	1.4	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 13; Fig. 12		-	1.65	2	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; Fig. 13; Fig. 12		-	1.19	1.5	mΩ
R_G	gate resistance	f = 1 MHz		-	1.1	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 75 A; V_{DS} = 15 V; V_{GS} = 10 V; Fig. 14; Fig. 15		-	243	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	222	-	nC
		I_D = 75 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 14; Fig. 15		-	118	-	nC
Q_{GS}	gate-source charge			-	39	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	22	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	17	-	nC
Q_{GD}	gate-drain charge			-	37	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 75 A; V_{DS} = 15 V; Fig. 14; Fig. 15		-	2.8	-	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{DS} = 15 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	14850	-	pF
C_{oss}	output capacitance			-	2799	-	pF
C_{rss}	reverse transfer capacitance			-	1215	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 0.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω; I_D = 75 A; T_j = 25 °C		-	95	-	ns
t_r	rise time	V_{DS} = 15 V; R_L = 0.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C; I_D = 75 A		-	213	-	ns
$t_{d(off)}$	turn-off delay time	V_{DS} = 15 V; R_L = 0.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω; I_D = 75 A; T_j = 25 °C		-	199	-	ns
t_f	fall time			-	115	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 15 V		-	67	-	ns
Q_r	recovered charge			-	123	-	nC

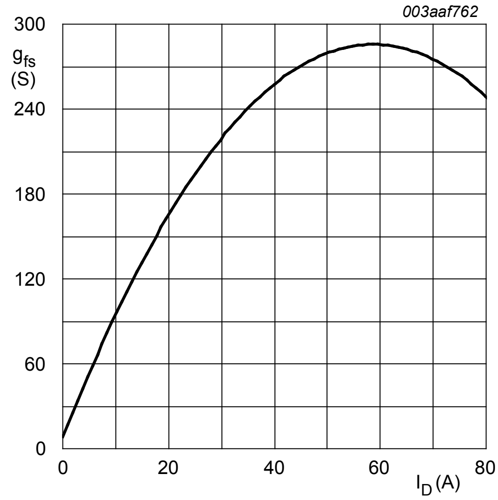


Fig. 5. Forward transconductance as a function of drain current; typical values

$$T_j = 25\,°C; V_{DS} = 15\,V$$

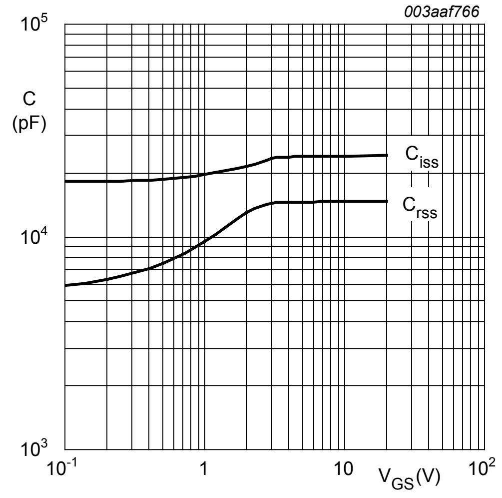


Fig. 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

$$V_{DS} = 0\,V; f = 1\,MHz$$

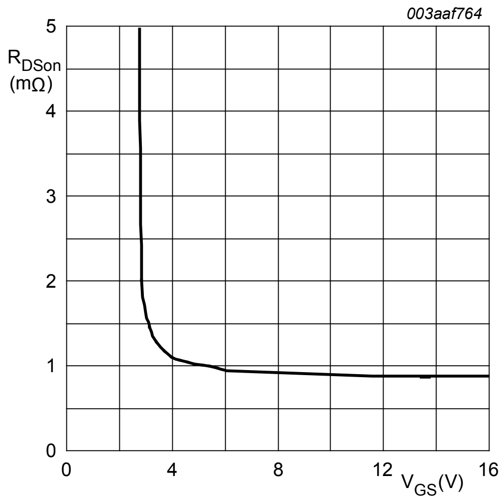


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\,°C; I_D = 25\,A$

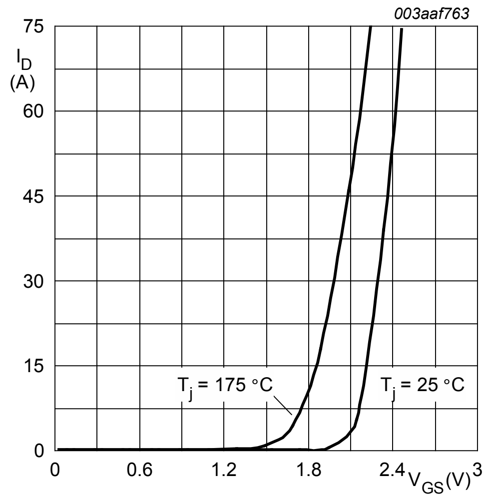


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} > I_D \times R_{DSon}$

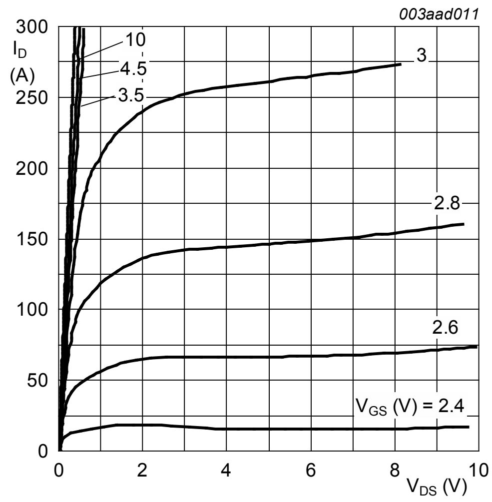


Fig. 9. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\,°C$

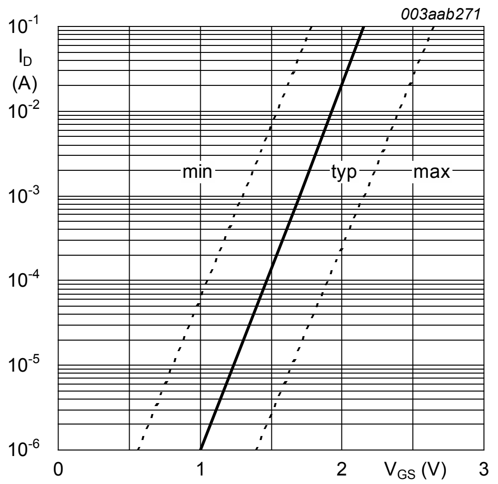


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\,°C; V_{DS} = 5\,V$

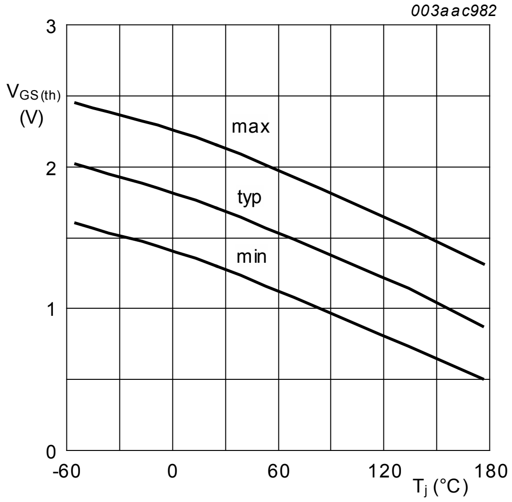


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1mA; V_{DS} = V_{GS}$$

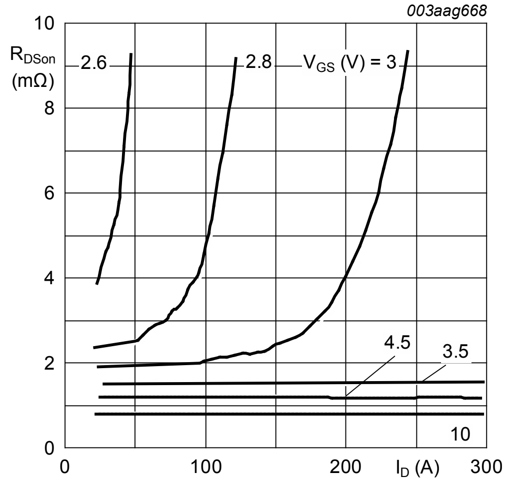


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25\,°C$$

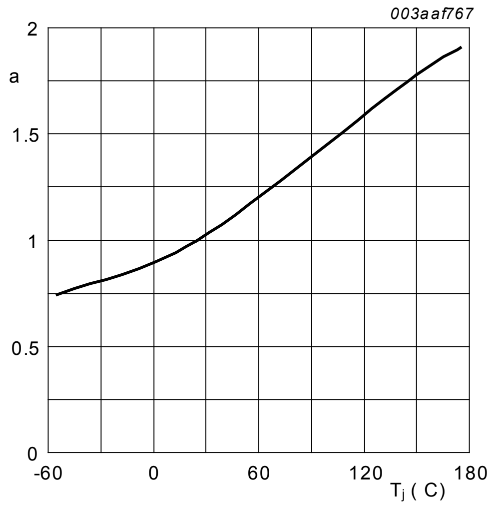


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

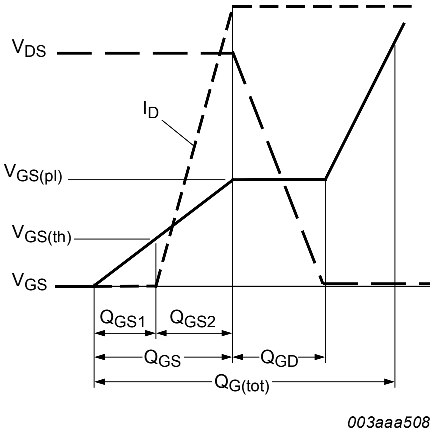


Fig. 14. Gate charge waveform definitions

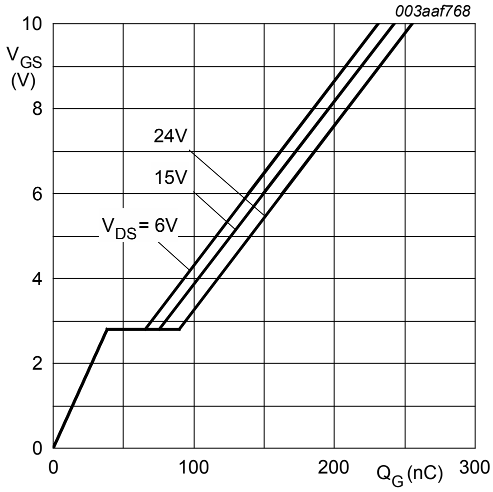


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25\ °C; I_D = 75\ A$

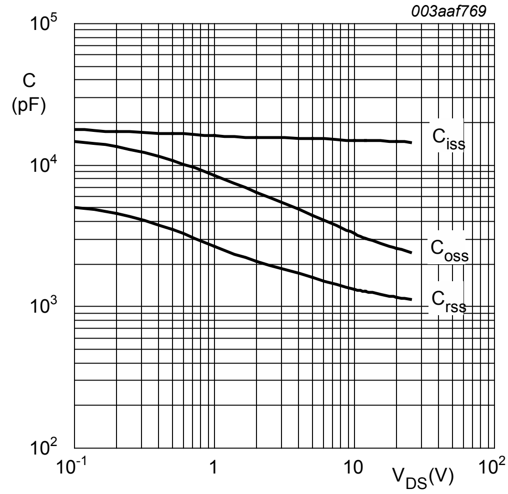


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

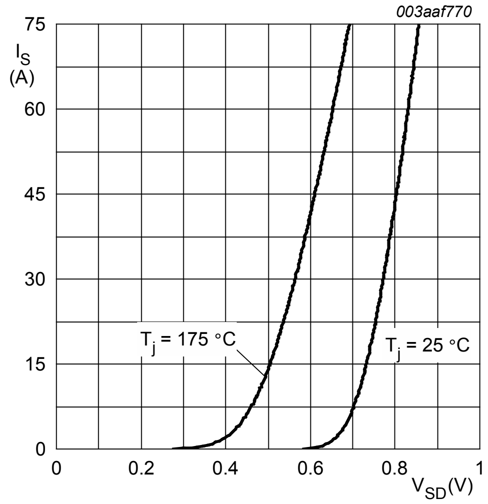
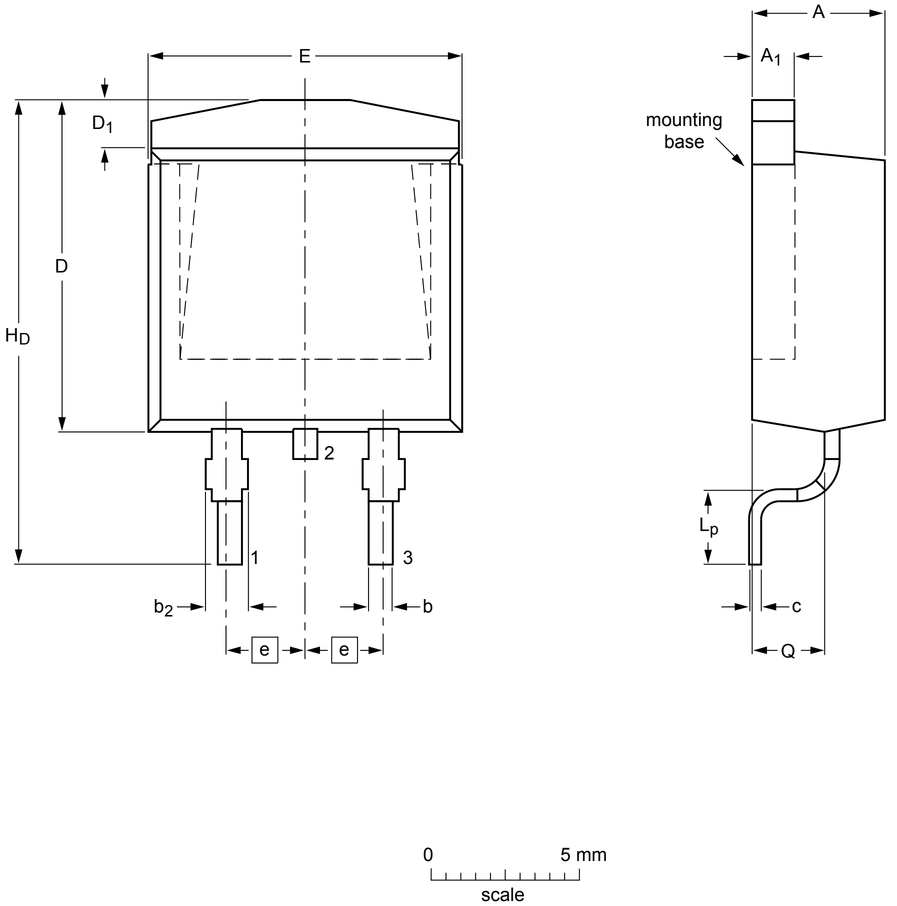


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\ V$

11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	b_2	c	D	D_1	E	e	H_D	L_p	Q
mm	max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
	nom									2.54			
	min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404_po

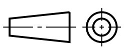
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT404						~~06-03-16~~ 13-02-25

Fig. 18. Package outline D2PAK (SOT404)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

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Date of release: 02 April 2014