IS31SE5001

IR SENSOR FOR TOUCHLESS PROXIMITY

GENERAL DESCRIPTION

The IS31SE5001 is a low-power, reflectance-based infrared light sensor with advanced signal processing and digital output. The sensor can detect making touchless motion possible.

The IS31SE5001 uses one infrared LED and an internal receiver which pick up the reflectance signal to perform touchless motion detection. When proximity motion happens, the flag bit in status register will be triggered and an interrupt signal is generated to inform the master to read the flag bit through I2C interface.

IS31SE5001 is available in QFN-8 (2mm × 2mm). It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

FEATURES

- Supply voltage from 2.7V~5.5V
- 400kHz I2C compatible interface
- 1µA shutdown current
- 0.6mA low supply current
- Detection range can be adjusted
- Integrated signal processing and digital output
- Auto interrupt clear
- Package in QFN-8 (2mm × 2mm)

APPLICATIONS

- Smart phones/GPS/MID/PAD/MP3
- Lighting/switch controller/ household electrical appliances
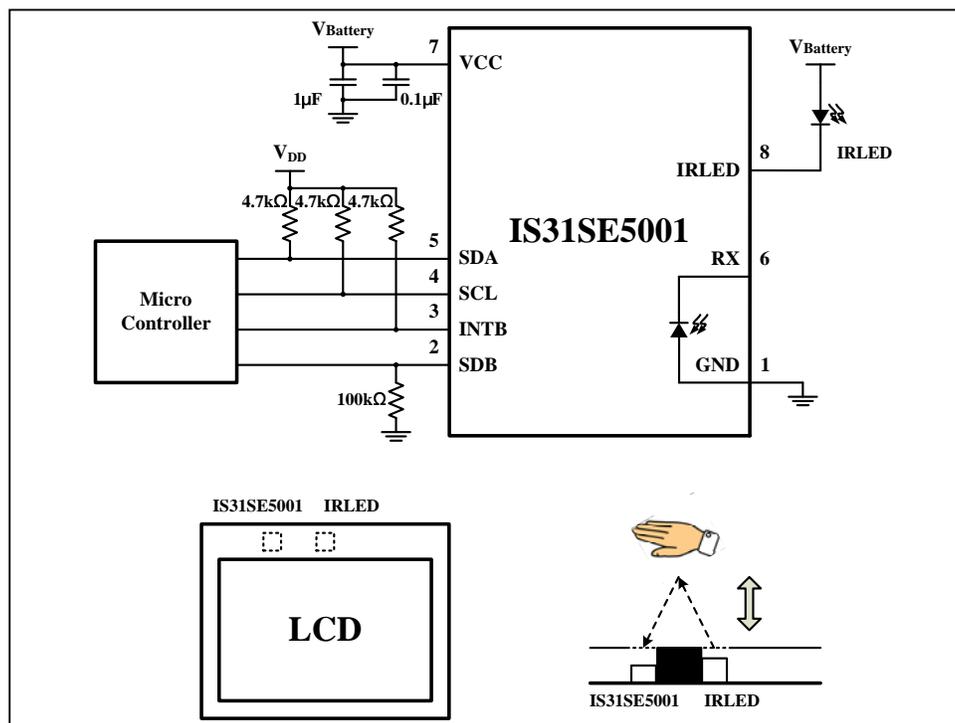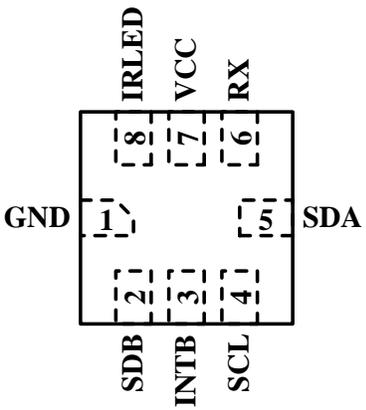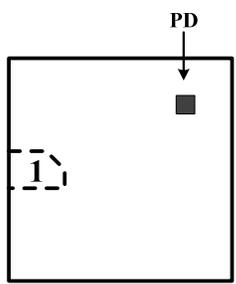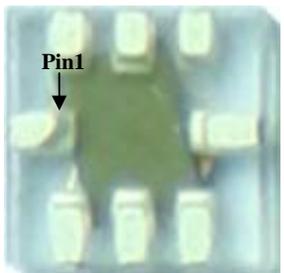- Toys/game machine

TYPICAL APPLICATION CIRCUIT

Figure 1   Typical Application Circuit

PIN CONFIGURATION

Package	Pin Configuration (Top View)	Scenograph (Top View)
QFN-8	IRLED / VCC / RX — pins 8, 7, 6; GND pin 1; SDA pin 5; SDB pin 2, INTB pin 3, SCL pin 4	PD
	Bottom View	**Top View**
Actual Picture	Pin1	Pin1 / PD
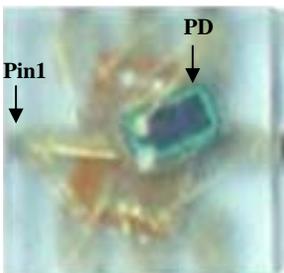
PIN DESCRIPTION

No.	Pin	Description
1	GND	Ground.
2	SDB	Shutdown pin, low active.
3	INTB	Interrupt signal, pulled down to inform master to read data.
4	SCL	The input for the I2C clock signal.
5	SDA	The input for the I2C data signal.
6	RX	Input signal of infrared LED receiver.
7	VCC	Power supply.
8	IRLED	IRLED emitting pin. Connect to IRLED.

IS31SE5001

ORDERING INFORMATION
Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31SE5001-QFLS2-TR	QFN-8, Lead-free	3000

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	$-0.3V \sim +6.0V$
Voltage at any input pin	$-0.3V \sim V_{CC}+0.3V$
Operating temperature range, T_A	$-40°C \sim +85°C$
Storage temperature range, T_{STG}	$-40°C \sim +85°C$

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 2.7V ~ 5.5V, unless otherwise noted. Typical value are T_A = +25°C, V_{CC} = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent current	V_{SDB} = V_{CC}		0.6		mA
I_{SD}	Shutdown current	V_{SDB} = 0V		1	3	µA
I_{IR}	Average current of IRLED	V_{LED} =3.6V(Note 1)		0.8		mA
I_P	Peak current of IRLED	EC = "0001" (Note 1,2)		400		mA
V_{INT}	INTB pin output voltage low	I_{OL} = 4mA			0.2	V
L	Maximum detect distance	EC = "0001" (Note 3)		15		cm
V_{IH}	Input logic high voltage	V_{CC} = 2.7V			0.4	V
V_{IL}	Input logic low voltage	V_{CC} = 5.5V	1.4			V

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			µs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			µs
$t_{SU, STA}$	Repeated START condition setup time		0.6			µs
$t_{SU, STO}$	STOP condition setup time		0.6			µs
$t_{HD, DAT}$	Data hold time				0.9	µs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			µs
t_{HIGH}	SCL clock high period		0.7			µs
t_R	Rise time of both SDA and SCL signals, receiving	(Note 4)		20+0.1Cb	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 4)		20+0.1Cb	300	ns

Note 1: Guaranteed by design.

Note 2: The EC bit is used to set emitting current. Please refer to the detailed information in Page 7.

Note 3: Because of different IRLED and material of cover, the detection distance will be different. The detail parameter should be tested. IR26-21C/L110/CT for IRLED is recommended.

Note 4: Cb = total capacitance of one bus line in pF. I_{SINK} ≤ 6mA. t_R and t_F measured between 0.3 × V_{CC} and 0.7 × V_{CC}.

DETAILED DESCRIPTION

I2C INTERFACE

The IS31SE5001 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31SE5001 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command.

The complete slave address is:

Table 1   Slave Address (Write only):

Bit	A7:A1	A0
Value	1010101	1/0

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31SE5001.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31SE5001's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31SE5001 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31SE5001, the register address byte is sent, most significant bit first. IS31SE5001 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31SE5001 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

READING PORT REGISTERS

To read the device data, the bus master must first send the IS31SE5001 address with the R/$\overline{\text{W}}$ bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the IS31SE5001 address with the R/$\overline{\text{W}}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31SE5001 to the master (Figure 5).

Figure 2   Interface timing
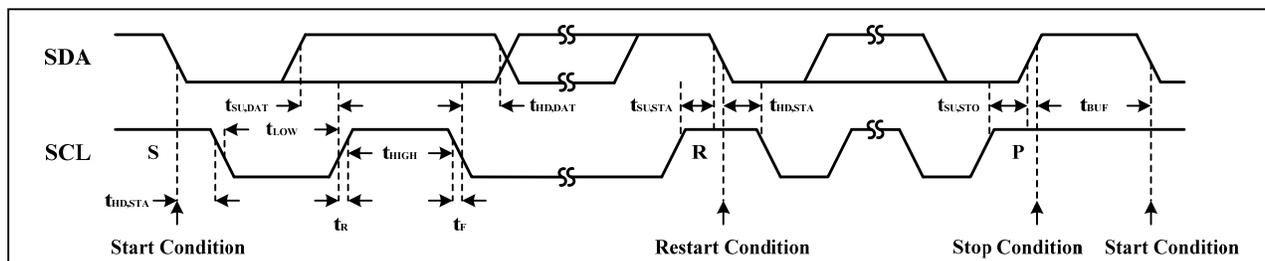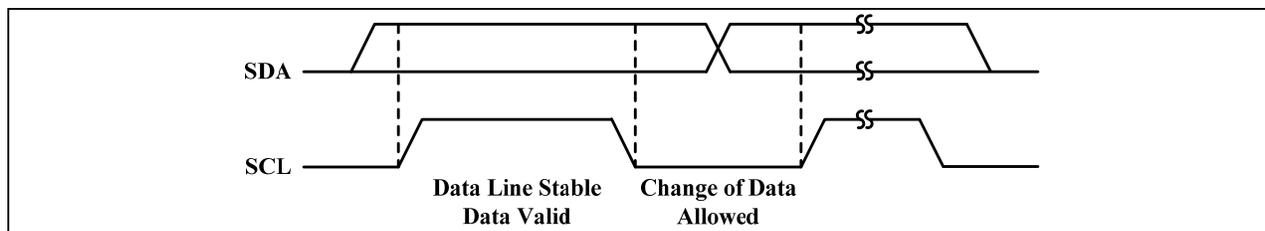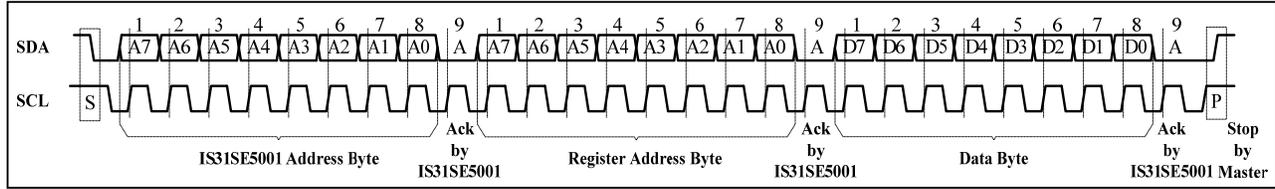

Figure 3   Bit transfer

Figure 4   Writing to IS31SE5001
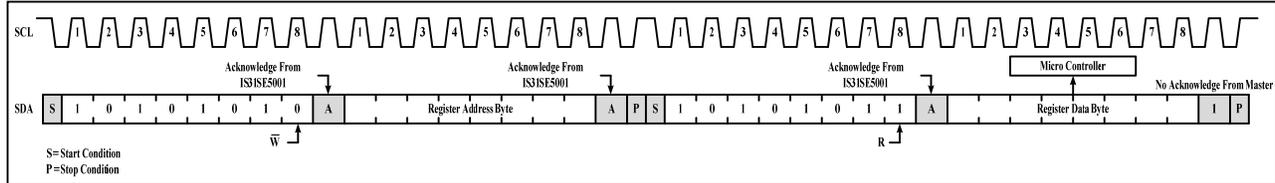
Figure 5   Reading from IS31SE5001

REGISTERS DEFINITIONS

Table 2   Register Function

Address	Name	Function	R/W	Table	Default
00h	Status Register	Store the motion information	R	3	xxxx xxxx
01h	Shutdown Register	Set software shutdown	W	4	0000 0000
11h	Configuration Register	Configure operating function	W	5	

Table 3   00h   Status Register (Read Only)

Bit	D7:D4	D3:D2	D1:D0
Name	-	PD	-
Default	-		

The Status Register stores the motion information which detected by IS31SE5001.

PD   Proximity Detection (Figure 6)
01   Be off
10   Be close
Others   No motion
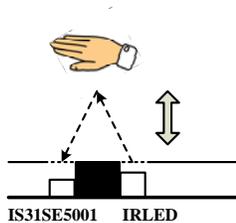

Figure 6   Proximity Detect (Side View)

Table 4   01h   Shutdown Register

Bit	D7:D1	D0
Name	-	SSD
Default	0000000	0

The Shutdown Register sets software shutdown mode of IS31SE5001.

SSD   Software Shutdown Enable
0   Software shutdown mode
1   Normal operation

Table 5   11h   Configuration Register

Bit	D7:D4	D3:D0
Name	-	EC
Default	0000	0000

The Configuration Register sets the operating function.

EC   Emitting Current Setting
(Adjusting detection distance, refer to detail information in Page 9)
0001   400mA
0011   280mA
0111   210mA
1111   70mA

Note the default value of EC is "0000". The EC bit must be configured when power on. The INTB pin will be triggered when configure the EC bit first time. This interrupt can be ignored.

FUNCTIONAL BLOCK DIAGRAM
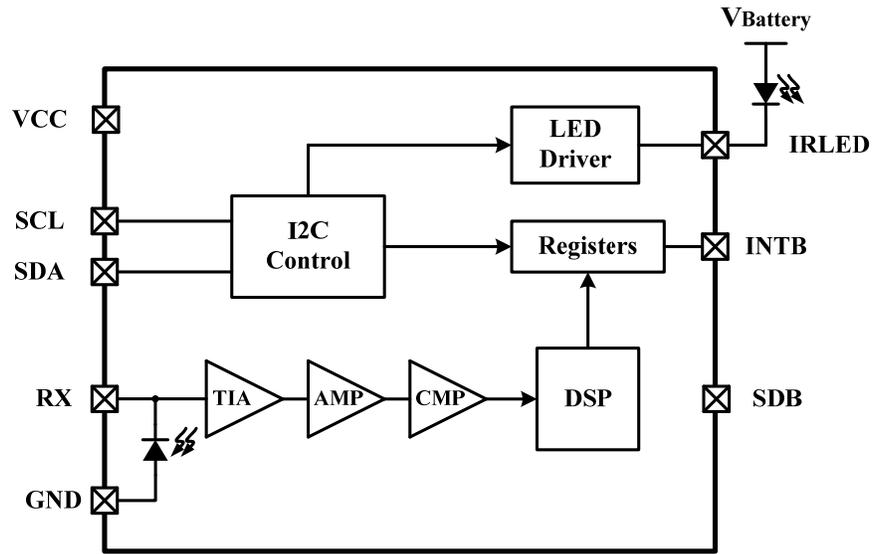
IS31SE5001

APPLICATION INFORMATION

GENERAL DESCRIPTION

The IS31SE5001 is a low-power, reflectance-based infrared light sensor with advanced signal processing and digital output. The sensor can detect making touchless motion possible.

STATUS INFORMATION

Master can get the current motion information by reading the PD bit of Status Register (00h).

The PD bit is available when IS31SE5001 operates. If the PD bit is "01", it means the object is away from the IC. If the PD bit is "10", it means the object is close to the IC (Table 3). If PD bit is other data, there is no motion.

INTERRUPTION

The changing of motion can be signed by the INTB pin. The INTB pin will be pulled low when object moving before the LCD panel (PD bit changing). And the MCU can get the information via reading the Status Register (00h). The INTB will be back to high until the MCU reading the Status Register (00h). The INTB pin will be high automatically when it stays low last 10ms to ensure system operating normally.

DETECTION DISTANCE

The emitting current can be adjusted by the EC bit of Configuration Register (11h). The larger current is, the longer distance detected.

Because of the different IRLED and material of cover, the detection distance will be different for the same emitting current. Detail information should be decided by testing.

In the stable mode and operating mode, the average emitting current for both two modes, I_{IR}, can be calculated by the Equation (1):

$$I_{IR} = \frac{1}{512} \times I_{EC} \qquad (1)$$

The I_{EC} is the emitting current which setting by the EC bit.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

SOFTWARE SHUTDOWN

By setting SSD bit of the Shutdown Register (01h) to "0", the IS31SE5001 will operate in software shutdown mode.

HARDWARE SHUTDOWN

The chip enters hardware shutdown mode when the SDB pin is pulled low, wherein they consume only 1μA (Typ.) current.

CLASSIFICATION REFLOW PROFILES

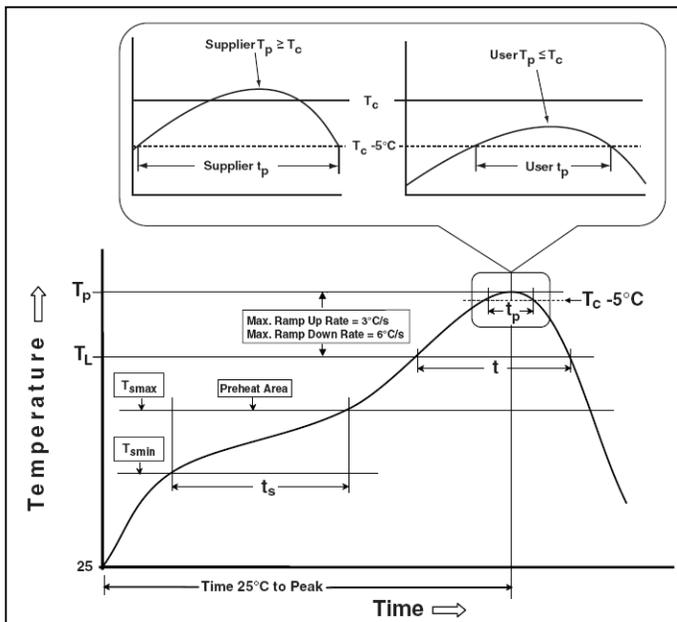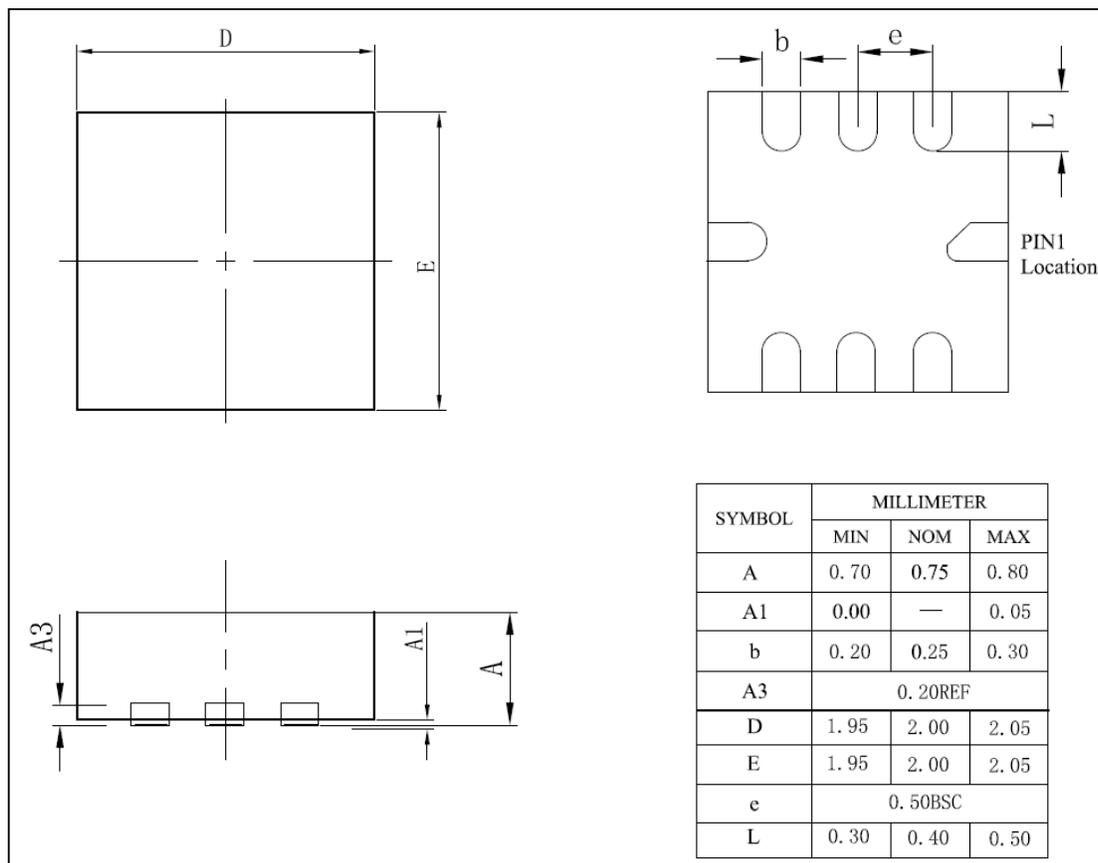| Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

Figure 7 Classification Profile

PACKAGE INFORMATION

QFN-8

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.20	0.25	0.30
A3	0.20REF		
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e	0.50BSC		
L	0.30	0.40	0.50

Note: All dimensions in millimeters unless otherwise stated.